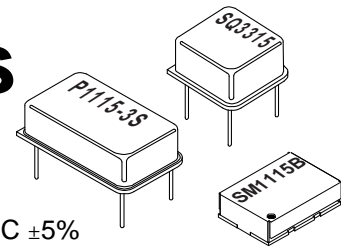




Tight Tolerance Series



- Full Size, Half Size or Leadless Surface Mount Clock Oscillator
- CMOS with Enable/ Disable, ± 15 PPM over Operating Temperature Range
- First Year Aging Rate of ± 3 PPM with ± 1 PPM per Year Thereafter at $25^\circ\text{C} \pm 5\%$
- Economic Alternative to TCXOs for Certain Applications

1.500 MHz – 69.999 MHz

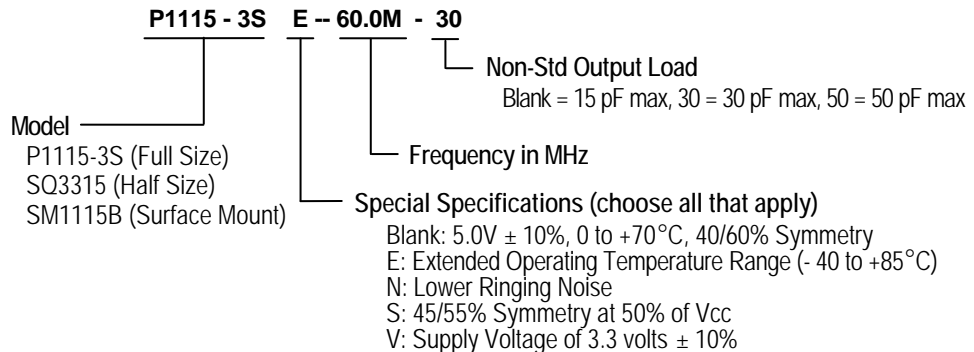
Standard Specifications

Overall Frequency Stability	± 15 PPM over Operating Temperature Range
Operating Temperature Range	-40 to $+85^\circ\text{C}$ or 0 to $+70^\circ\text{C}$ available
Supply Voltage (Vcc)	5.0 volts and 3.3 volts available
Symmetry (Duty Cycle)	40/60 to 60/40% is standard, but 45/55% at 50% of Vcc is also available (see Waveform 1)
Logic Levels	Logic "1" 90% of Vcc MIN; Logic "0" 10% of Vcc MAX
Output Load	Standard load is 15 pF maximum, see Test Circuit 3 (consult factory for heavier loads)
Ringing Noise	Depends on frequency and output load. See EMI application note
Supply Current (Icc)	Depends on frequency and output load. See SQ3345 Series specification
Rise and Fall Time (Tr & Tf)	Depends on frequency and output load. See SQ3345 Series specification
Enable/Disable Option (E/D)	Output enabled when Pin #1 is open or at Logic "1"; Output disabled when Pin #1 is at Logic "0".

Part Numbering Guide

Packaging

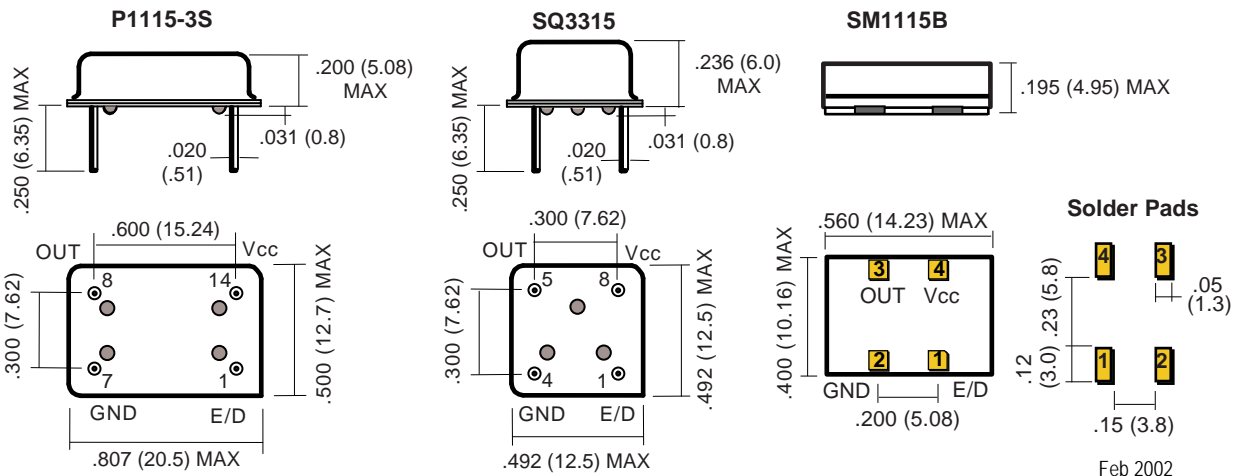
Thru-Hole: Tubes or on Pads,
Surface Mount: Tubes or
24mm tape
16mm pitch



Consult factory for available frequencies and specs. Not all options available for all frequencies. A special part number may be assigned.
Frequency Stability is inclusive of frequency shifts due to calibration, temperature, supply voltage, shock, vibration and load

Mechanical: inches (mm) not to scale

Due to part size and factory abilities, part marking may vary from lot to lot and may contain our part number or an internal code.



Feb 2002