

## Power MOSFET

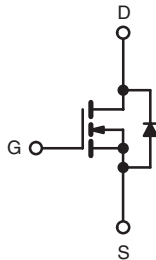
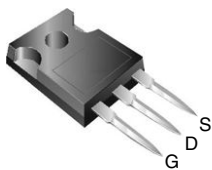
| PRODUCT SUMMARY            |                      |
|----------------------------|----------------------|
| $V_{DS}$ (V) at $T_J$ max. | 560 V                |
| $R_{DS(on)}$ ( $\Omega$ )  | $V_{GS} = 10$ V 0.38 |
| $Q_g$ (Max.) (nC)          | 68                   |
| $Q_{gs}$ (nC)              | 17.6                 |
| $Q_{gd}$ (nC)              | 21.8                 |
| Configuration              | Single               |

### FEATURES

- Low Figure-of-Merit  $R_{on} \times Q_g$
- 100 % Avalanche Tested
- Gate Charge Improved
- $T_{rr}/Q_{rr}$  Improved
- Compliant to RoHS Directive 2002/95/EC



Available  
**RoHS\***  
COMPLIANT

**TO-247AC**


N-Channel MOSFET

| ORDERING INFORMATION |               |
|----------------------|---------------|
| Package              | TO-247AC      |
| Lead (Pb)-free       | SiHG16N50C-E3 |

| ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted |                  |                |      |   |
|--|------------------|----------------|------|---|
| PARAMETER  | SYMBOL           | LIMIT          | UNIT |   |
| Drain-Source Voltage   | $V_{DS}$         | 500            | V    |   |
| Gate-Source Voltage  | $V_{GS}$         | $\pm 30$       |      |   |
| Continuous Drain Current ( $T_J = 150$ °C) <sup>a</sup>        | $V_{GS}$ at 10 V | $T_C = 25$ °C  | 16   | A |
|  |                  | $T_C = 100$ °C | 10   |   |
| Pulsed Drain Current <sup>c</sup>                              | $I_{DM}$         | 40             |      |   |
| Linear Derating Factor   |                  | 2              | W/°C |   |
| Single Pulse Avalanche Energy <sup>b</sup>                     | $E_{AS}$         | 320            | mJ   |   |
| Maximum Power Dissipation                                      | $P_D$            | 250            | W    |   |
| Operating Junction and Storage Temperature Range               | $T_J, T_{stg}$   | - 55 to + 150  | °C   |   |
| Soldering Recommendations (Peak Temperature) <sup>d</sup>      | for 10 s         | 300            |      |   |

### Notes


- Limited by maximum junction temperature.
- $V_{DD} = 50$  V, starting  $T_J = 25$  °C,  $L = 2.5$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 16$  A.
- Repetitive rating; pulse width limited by maximum junction temperature.
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

**THERMAL RESISTANCE RATINGS**

| PARAMETER                        | SYMBOL     | TYP. | MAX. | UNIT |
|----------------------------------|------------|------|------|------|
| Maximum Junction-to-Ambient      | $R_{thJA}$ | -    | 40   | °C/W |
| Maximum Junction-to-Case (Drain) | $R_{thJC}$ | -    | 0.5  |      |

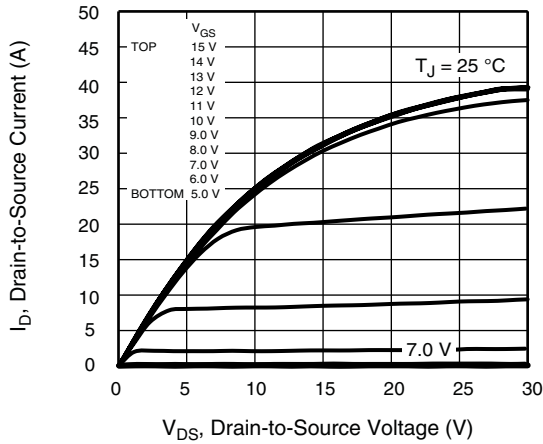
**SPECIFICATIONS**  $T_J = 25\text{ °C}$ , unless otherwise noted

| PARAMETER                                      | SYMBOL              | TEST CONDITIONS  | MIN. | TYP.  | MAX.      | UNIT          |
|--|---------------------|--|------|-------|-----------|---------------|
| <b>Static</b>                                  |                     |  |      |       |           |               |
| Drain-Source Breakdown Voltage                 | $V_{DS}$            | $V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$  | 500  | -     | -         | V             |
| $V_{DS}$ Temperature Coefficient               | $\Delta V_{DS}/T_J$ | Reference to $25\text{ °C}$ , $I_D = 1\text{ mA}$  | -    | 0.6   | -         | V/°C          |
| Gate-Source Threshold Voltage (N)              | $V_{GS(th)}$        | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$  | 3.0  | -     | 5.0       | V             |
| Gate-Source Leakage                            | $I_{GSS}$           | $V_{GS} = \pm 30\text{ V}$   | -    | -     | $\pm 100$ | nA            |
| Zero Gate Voltage Drain Current                | $I_{DSS}$           | $V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$   | -    | -     | 50        | $\mu\text{A}$ |
|  |                     | $V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ °C}$  | -    | -     | 250       |               |
| Drain-Source On-State Resistance               | $R_{DS(on)}$        | $V_{GS} = 10\text{ V}, I_D = 8\text{ A}$   | -    | 0.317 | 0.38      | $\Omega$      |
| Forward Transconductance <sup>a</sup>          | $g_{fs}$            | $V_{DS} = 50\text{ V}, I_D = 3\text{ A}$   | -    | 3     | -         | S             |
| <b>Dynamic</b>                                 |                     |  |      |       |           |               |
| Input Capacitance                              | $C_{iss}$           | $V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$  | -    | 1900  | -         | $\mu\text{F}$ |
| Output Capacitance                             | $C_{oss}$           |  | -    | 230   | -         |               |
| Reverse Transfer Capacitance                   | $C_{rss}$           |  | -    | 24    | -         |               |
| Total Gate Charge                              | $Q_g$               | $V_{GS} = 10\text{ V}, I_D = 16\text{ A}, V_{DS} = 400\text{ V}$   | -    | 45    | 68        | nC            |
| Gate-Source Charge                             | $Q_{gs}$            |  | -    | 18    | -         |               |
| Gate-Drain Charge                              | $Q_{gd}$            |  | -    | 22    | -         |               |
| Turn-On Delay Time                             | $t_{d(on)}$         | $V_{DD} = 250\text{ V}, I_D = 16\text{ A}, R_g = 9.1\text{ }\Omega, V_{GS} = 10\text{ V}$  | -    | 27    | -         | ns            |
| Rise Time                                      | $t_r$               |  | -    | 156   | -         |               |
| Turn-Off Delay Time                            | $t_{d(off)}$        |  | -    | 29    | -         |               |
| Fall Time                                      | $t_f$               |  | -    | 31    | -         |               |
| Gate Input Resistance                          | $R_g$               | $f = 1\text{ MHz}, \text{open drain}$  | -    | 1.6   | -         | $\Omega$      |
| <b>Drain-Source Body Diode Characteristics</b> |                     |  |      |       |           |               |
| Continuous Source-Drain Diode Current          | $I_S$               | MOSFET symbol showing the integral reverse p - n junction diode  | -    | -     | 16        | A             |
| Pulsed Diode Forward Current                   | $I_{SM}$            |  | -    | -     | 30        |               |
| Body Diode Voltage                             | $V_{SD}$            | $T_J = 25\text{ °C}, I_S = 10\text{ A}, V_{GS} = 0\text{ V}$   | -    | -     | 1.8       | V             |
| Body Diode Reverse Recovery Time               | $t_{rr}$            | $T_J = 25\text{ °C}, I_F = I_S, dI/dt = 100\text{ A}/\mu\text{s}, V_R = 20\text{ V}$   | -    | 555   | -         | ns            |
| Body Diode Reverse Recovery Charge             | $Q_{rr}$            |  | -    | 5.5   | -         | $\mu\text{C}$ |
| Body Diode Reverse Recovery Current            | $I_{RRM}$           |  | -    | 18    | -         | A             |

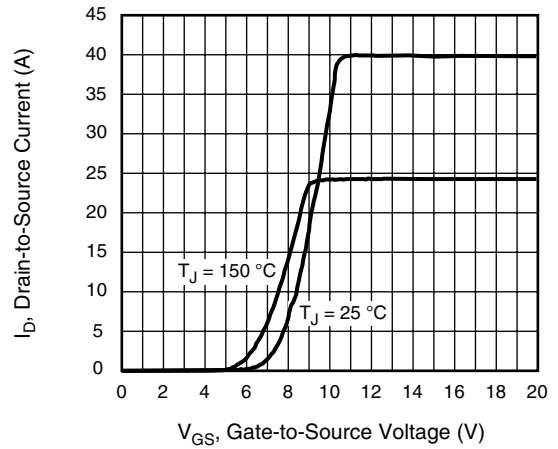
**Note**

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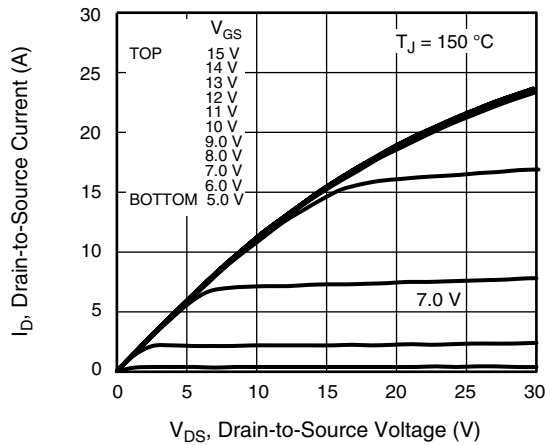
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



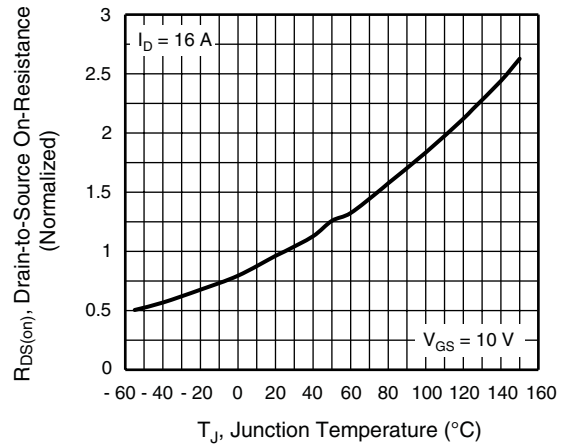
**Fig. 1 - Typical Output Characteristics**



**Fig. 3 - Typical Transfer Characteristics**



**Fig. 2 - Typical Output Characteristics**



**Fig. 4 - Normalized On-Resistance vs. Temperature**

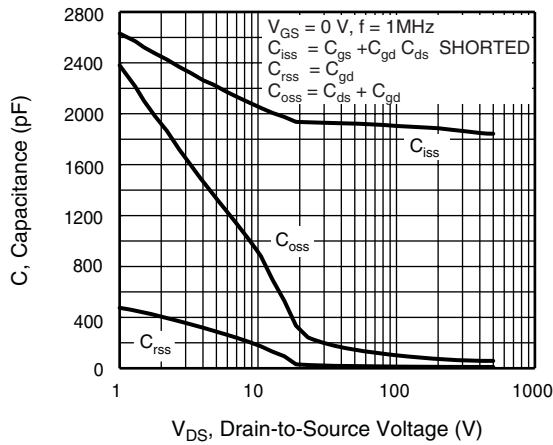


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

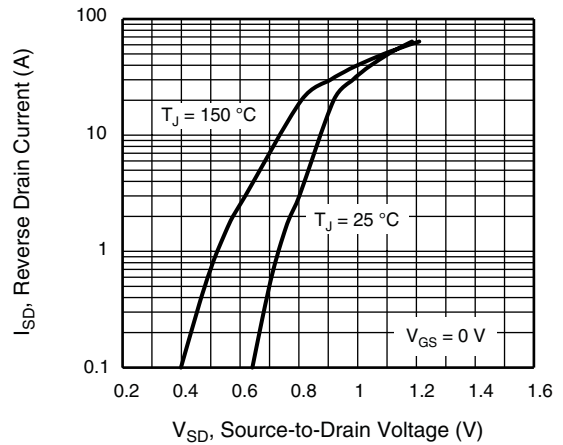


Fig. 7 - Typical Source-Drain Diode Forward Voltage

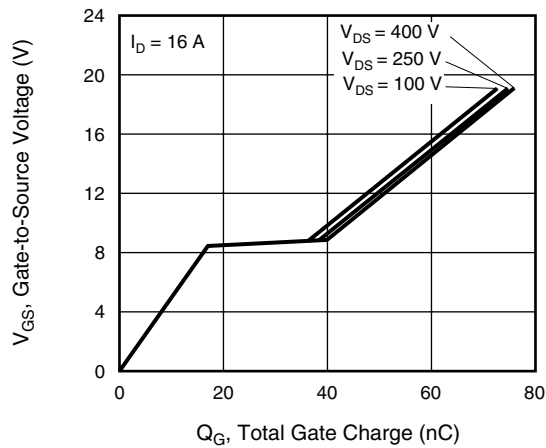


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

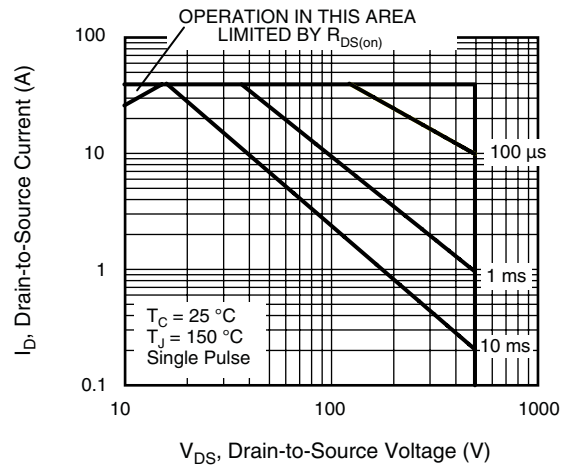


Fig. 8 - Maximum Safe Operating Area

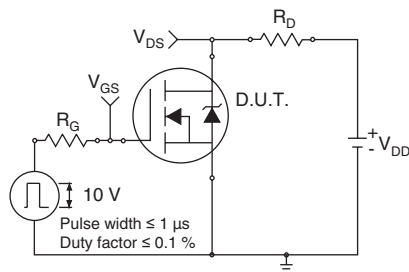


Fig. 9a - Switching Time Test Circuit

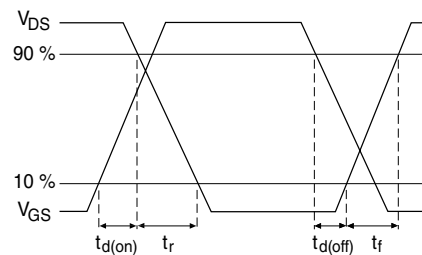
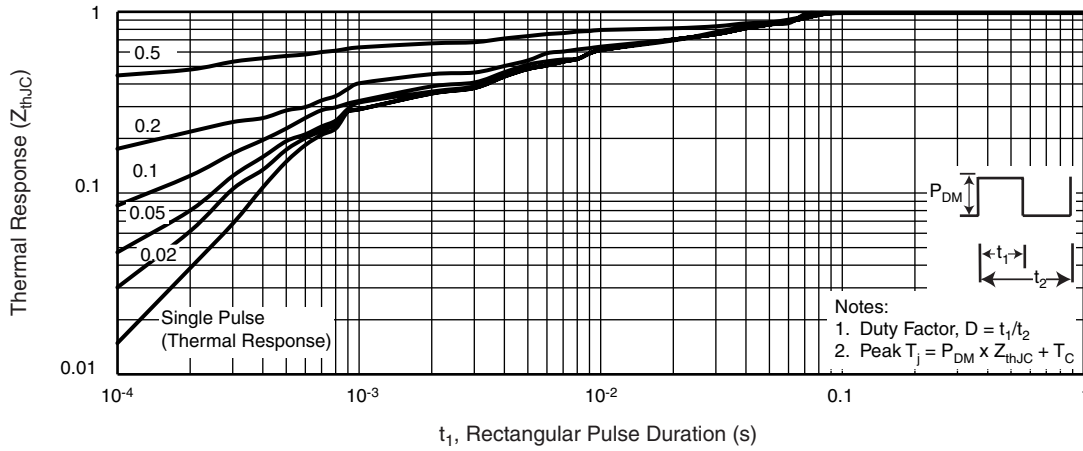
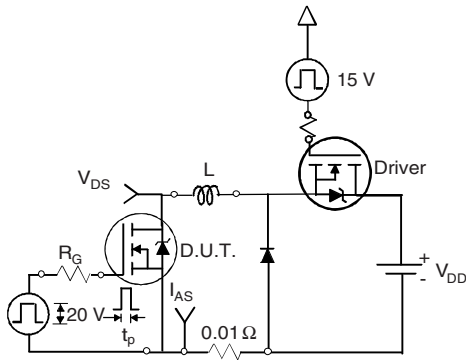


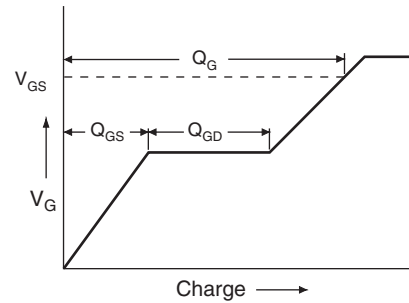
Fig. 9b - Switching Time Waveforms



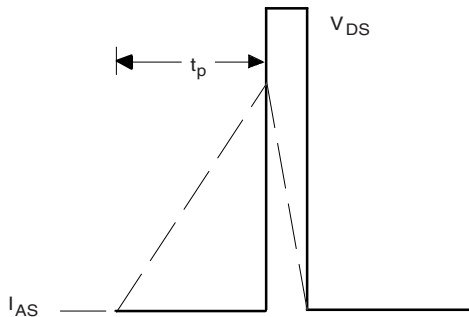
**Fig. 10 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**



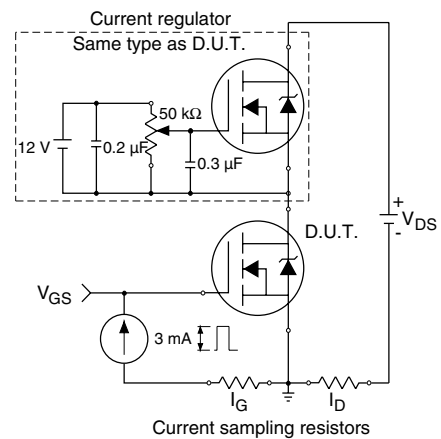
**Fig. 11a - Unclamped Inductive Test Circuit**



**Fig. 12a - Basic Gate Charge Waveform**

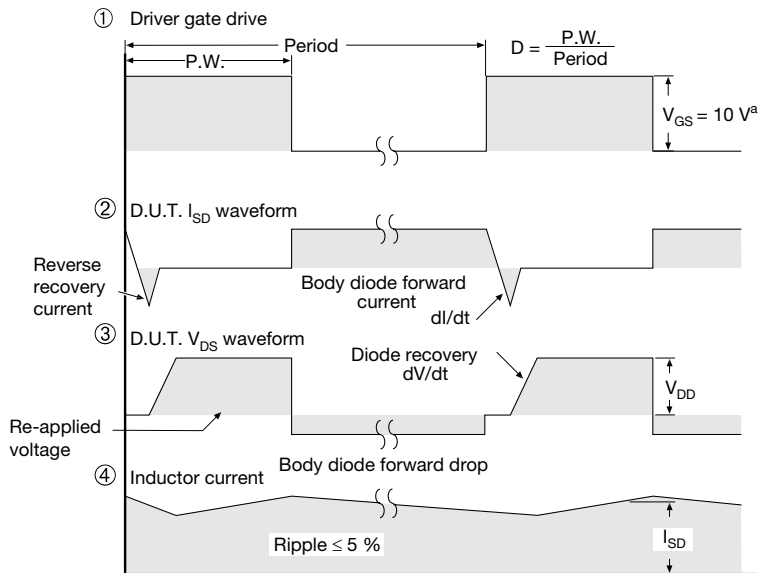
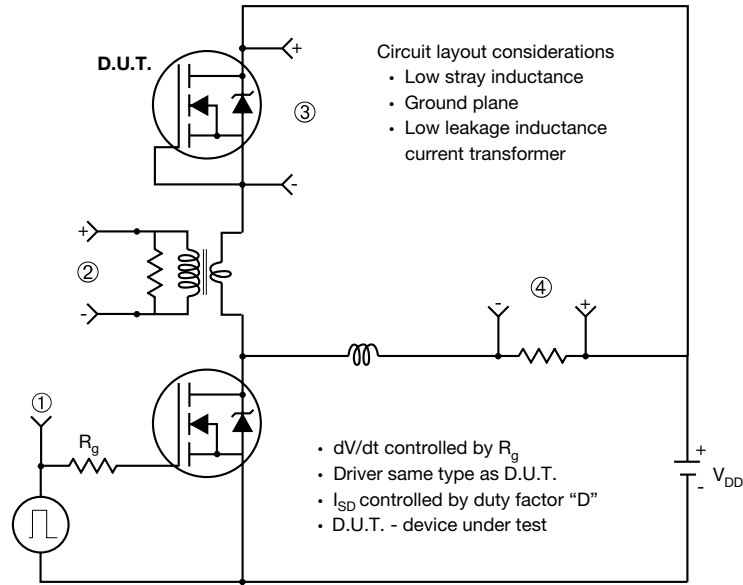


**Fig. 11b - Unclamped Inductive Waveforms**



**Fig. 12b - Gate Charge Test Circuit**

Peak Diode Recovery dV/dt Test Circuit



Note

a.  $V_{GS} = 5 V$  for logic level devices

Fig. 13 - For N-Channel

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