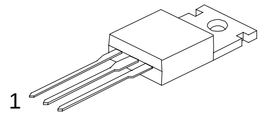
NPN SILICON POWER TRANSISTORS



TO-220

*Pb-free plating product number: MJE13003L

■ DESCRIPTION

These devices are designed for high–voltage, high–speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220V SWITCHMODE .

■ FEATURES

* Reverse Biased SOA with Inductive Load @ Tc=100℃
* Inductive Switching Matrix 0.5 ~ 1.5 Amp, 25 and 100℃
  Typical tc = 290ns @ 1A, 100℃.
* 700V Blocking Capability

■ APPLICATIONS

* Switching Regulator's, Inverters
* Motor Controls
* Solenoid/Relay drivers
* Deflection circuits

■ ORDERING INFORMATION

Order Number		Package	Pin Assignment			Packing
Normal	Lead Free Plating		1	2	3	
MJE13003-x-TA3-F-T	MJE13003L-x-TA3-F-T	TO-220	B	C	E	Tube

Note: x: Rank, refer to Classification of h_{FE1}.

MJE13003L-x-TA3-F-T

(1)Packing Type	(1)T: Tube
(2)Pin Assignment	(2) refer to Pin Assignment
(3)Package Type	(3) TA3: TO-220
(4)Rank	(4) x: refer to Classification of h_{FE1}
(5)Lead Plating	(5) L: Lead Free Plating, Blank: Pb/Sn

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATINGS	UNIT
Collector-Emitter Voltage		$V_{CEO(SUS)}$	400	V
Collector-Emitter Voltage		V_{CEO}	700	V
Emitter Base Voltage		V_{EBO}	9	V
Collector Current	Continuous	I_C	1.5	A
	Peak (1)	I_{CM}	3	
Base Current	Continuous	I_B	0.75	A
	Peak (1)	I_{BM}	1.5	
Emitter Current	Continuous	I_E	2.25	A
	Peak (1)	I_{EM}	4.5	
Total Power Dissipation @ Ta=25℃		P_D	1.4	W
Derate above 25℃			11.2	mW/℃
Total Power Dissipation @ T_C=25℃		P_D	40	W
Derate above 25℃			320	mW/℃
Junction Temperature		T_J	150	℃
Storage Temperature		T_{STG}	-40 ~ +150	℃

Note Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	89	℃/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.12	℃/W

(1) Pulse Test: Pulse Width=5ms, Duty Cycle≤10%

■ ELECTRICAL CHARACTERISTICS (T_C=25°C, unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS (Note)						
Collector-Emitter Sustaining Voltage	$V_{CEO(SUS)}$	I_C=10 mA , I_B=0	400			V
Collector Cutoff Current	I_{CEO}	V_{CEO}=Rated Value, $V_{BE(OFF)}$=1.5 V, T_C=25°C			1	mA
		V_{CEO}=Rated Value, $V_{BE(OFF)}$=1.5 V, T_C=100℃			5	
Emitter Cutoff Current	I_{EBO}	V_{EB}=9 V, I_C=0			1	mA
SECOND BREAKDOWN						
Second Breakdown Collector Current with bass forward biased	Is/b			See Figure 5		
Clamped Inductive SOA with base reverse biased	RBSOA			See Figure 6		
ON CHARACTERISTICS (Note)						
DC Current Gain	h_{FE1}	I_C=0.5A, V_{CE}=2V	8		40	
	h_{FE2}	I_C=1A, V_{CE}=2V	5		25	
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C=0.5A, I_B=0.1A			0.5	V
		I_C=1A, I_B=0.25A			1	
		I_C=1.5A, I_B=0.5A			3	
		I_C=1A, I_B=0.25A, T_C=100℃			1	
Base-Emitter Saturation Voltage	$V_{BE(SAT)}$	I_C=0.5A, I_B=0.1A			1	V
		I_C=1A, I_B=0.25A			1.2	
		I_C=1A, I_B=0.25A, T_C=100℃			1.1	
DYNAMIC CHARACTERISTICS						
Current-Gain-Bandwidth Product	f_T	I_C=100mA, V_{CE}=10V, f=1MHz	4	10		MHz
Output Capacitance	Cob	V_{CB}=10V, I_E=0, f=0.1MHz		21		pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	t_D	V_{CC}=125V, I_C=1A, I_{B1}=I_{B2}=0.2A, t_P=25μs, Duty Cycle≤1%		0.05	0.1	μs
Rise Time	t_R			0.5	1	μs
Storage Time	t_S			2	4	μs
Fall Time	t_{FALL}			0.4	0.7	μs

■ ELECTRICAL CHARACTERISTICS(Cont.)

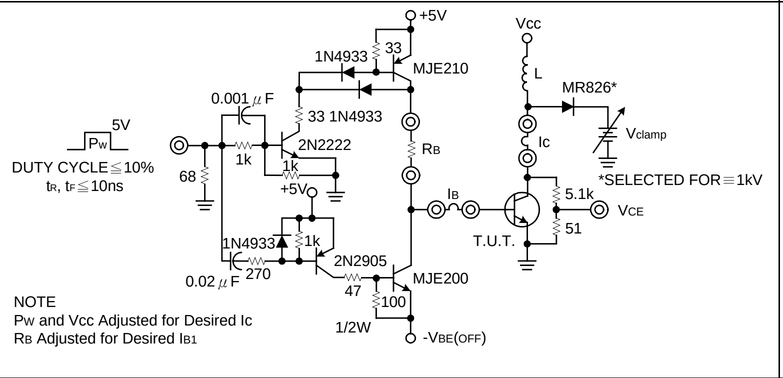
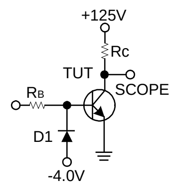
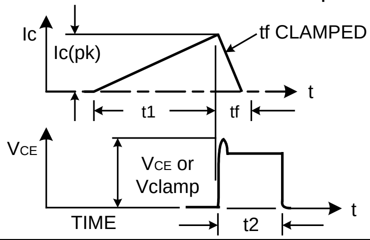
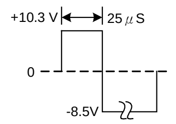
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Inductive Load, Clamped (Table 1)						
Storage Time	t_{SV}	I_C=1A, Vclamp=300V, I_{B1}=0.2A, $V_{BE(OFF)}$=5Vdc, T_C=100℃		1.7	4	μs
Crossover Time	t_C			0.29	0.75	μs
Fall Time	t_{FALL}			0.15		μs

Note: Pulse Test : PW=300μs, Duty Cycle≤2%

■ CLASSIFICATION OF h_{FE1}

RANK	A	B	C	D	E	F
RANGE	8 ~ 16	15 ~ 21	20 ~ 26	25 ~ 31	30 ~ 36	35 ~ 40

Table 1.Test Conditions for Dynamic Performance

	Reverse Bias Safe Operating Area and Inductive Switching	Resistive Switching
Test Circuits		
Circuit Values	Coil Data : GAP for 30 mH/2 A V_{CC}=20V Ferroxcube core #6656 Lcoil=50mH Vclamp=300V Full Bobbin (~ 200 Turns) #20	V_{CC}=125V R_C=125Ω D1=1N5820 or Equiv. R_C=47Ω
Test Waveforms	Output Waveforms  t1 Adjusted to Obtain Ic t1 Lcoil(Icpk) / Vcc t2 Lcoil(Icpk) / Vclamp Test Equipment Scope-Tektronics 475 or Equivalent	 tr, tf<10ns Duty Cycly=1.0% RB and Rc adjusted for desired IB and Ic

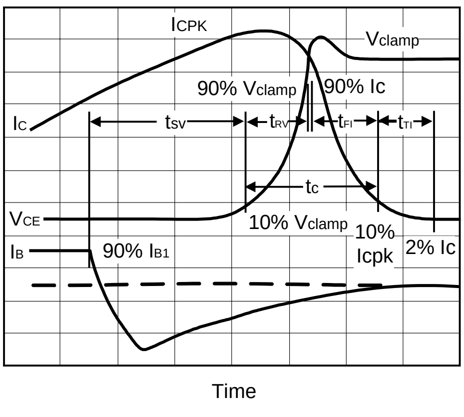


Figure 1. Inductive Switching Measurements

Table 2. Typical Inductive Switching Performance

Ic AMP	Tc ℃	tsv μs	t_{RV} μs	t_{FI} μs	t_{TI} μs	tc μs
0.5	25 100	1.3 1.6	0.23 0.26	0.30 0.30	0.35 0.40	0.30 0.36
1	25 100	1.5 1.7	0.10 0.13	0.14 0.26	0.05 0.06	0.16 0.29
1.5	25 100	1.8 3	0.07 0.08	0.10 0.22	0.05 0.08	0.16 0.28

NOTE: All Data Recorded in the Inductive Switching Circuit in Table 1

■ SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads, which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{SV} = Voltage Storage Time, 90% I_{B1} to 10% Vclamp
t_{RV} = Voltage Rise Time, 10 ~ 90% Vclamp
t_{FI}= Current Fall Time, 90 ~ 10% I_C
t_{TI} = Current Tail, 10 ~ 2% I_C
t_C = Crossover Time, 10% Vclamp to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these Terms. For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN–222:

$PSWT = 1/2\ V_{CC}I_C(t_C)f$

In general, $t_{RV} + t_{FI} \approx t_C$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25℃ and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_C and t_{SV}) which are guaranteed at 100℃.

RESISTIVE SWITCHING PERFORMANCE

Figure 2. Turn-On Time

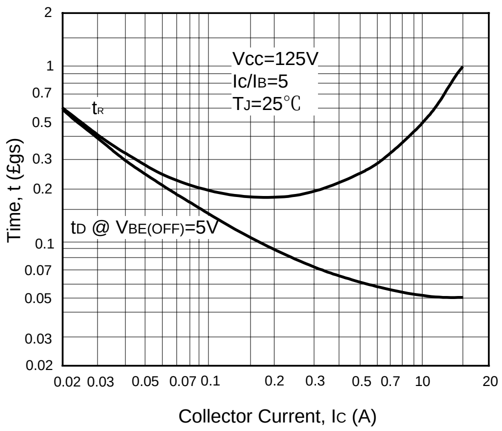


Figure 3. Turn-Off Time

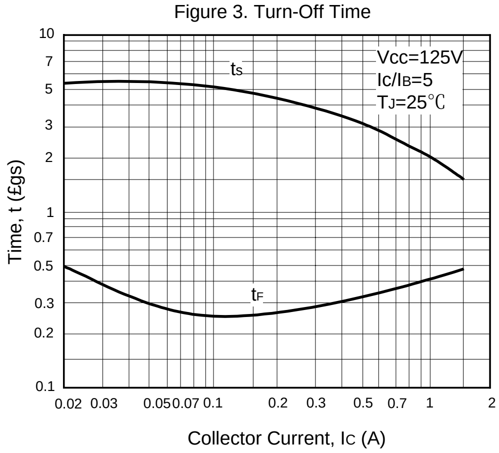
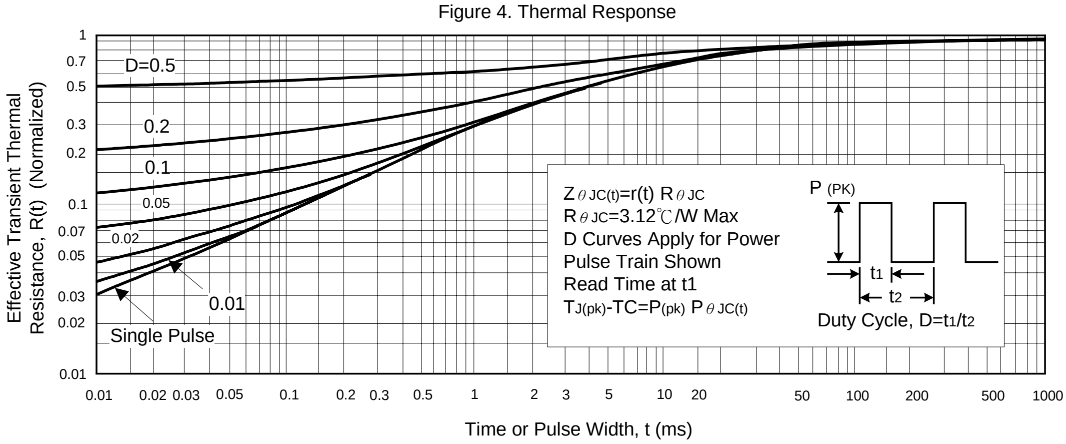


Figure 4. Thermal Response



■ SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on T_C = 25℃; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C≥25℃. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 5 may be found at any case temperature by using the appropriate curve on Figure 7.

$T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 6 gives PBSOA characteristics.

The Safe Operating Area of figures 5 and 6 are specified ratings (for these devices under the test conditions shown.)

Figure 5. Active Region Safe Operating Area

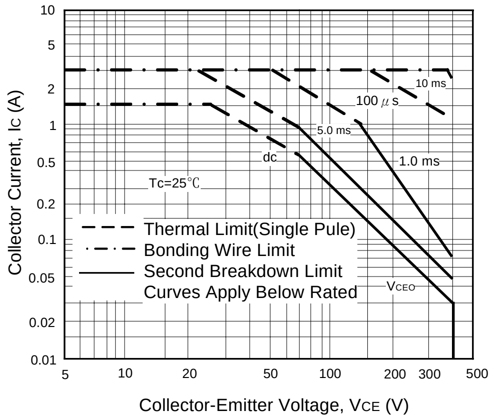


Figure 6. Reverse Bias Safe Operating Area

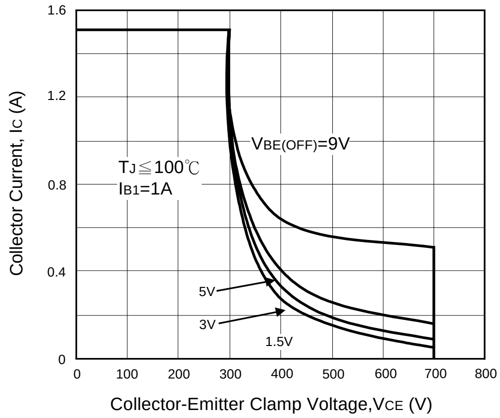
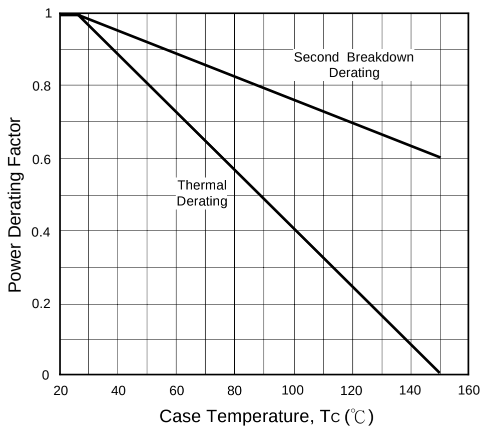
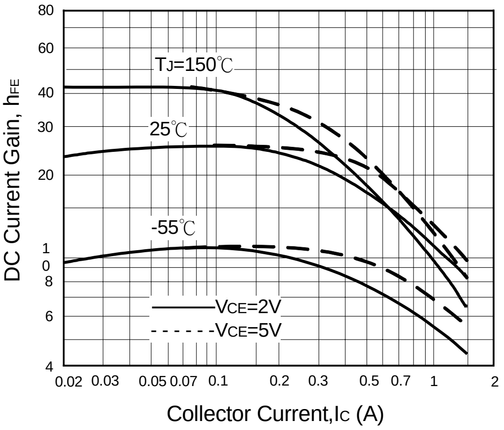


Figure 7. Forward Bias Power Derating

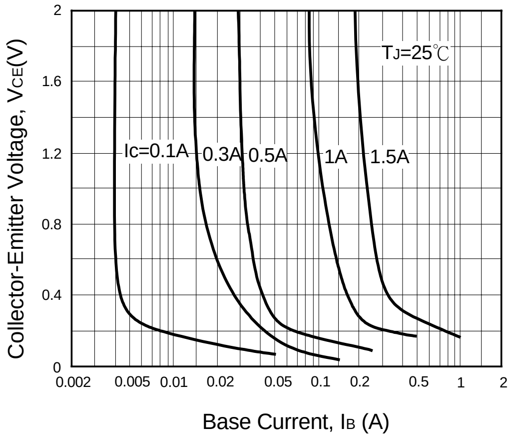


■ TYPICAL PERFORMANCE CHARACTERISTICS

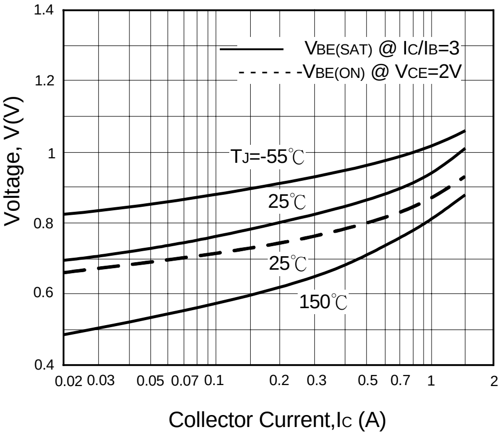
DC Current Gain



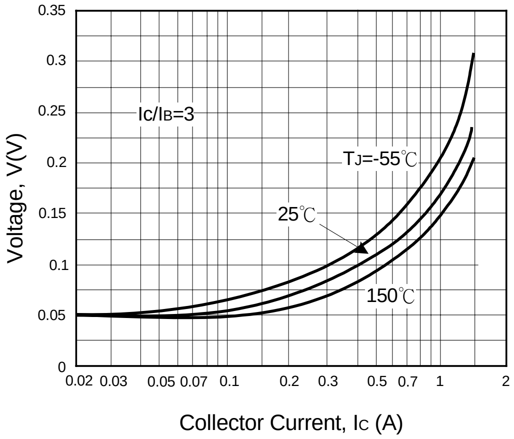
Collector Saturation Region



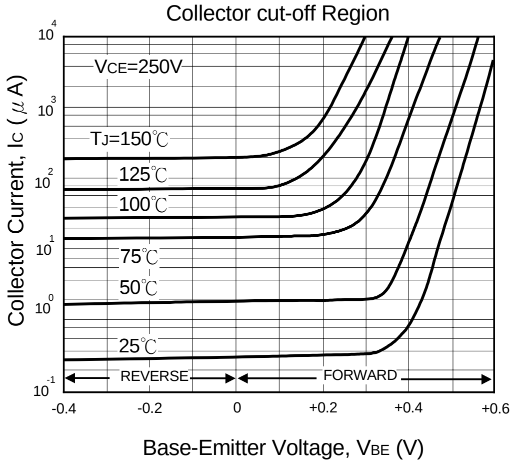
Base-Emitter Voltage



Collector-Emitter Saturation Region



Collector cut-off Region



Capacitance