

TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (π -MOSIII)

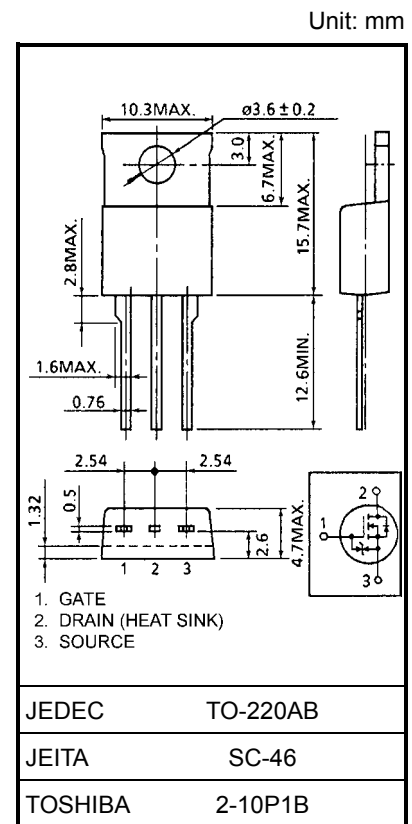
2SK2608

Switching Regulator Applications

- Low drain-source ON resistance : $R_{DS(ON)} = 3.73 \Omega$ (typ.)
- High forward transfer admittance : $|Y_{fs}| = 2.6 S$ (typ.)
- Low leakage current : $I_{DSS} = 100 \mu A$ (max) ($V_{DS} = 720 V$)
- Enhancement-mode : $V_{th} = 2.0 \sim 4.0 V$ ($V_{DS} = 10 V, I_D = 1 mA$)

Maximum Ratings ($T_a = 25^\circ C$)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	900	V
Drain-gate voltage ($R_{GS} = 20 k\Omega$)		V_{DGR}	900	V
Gate-source voltage		V_{GSS}	± 30	V
Drain current	DC (Note 1)	I_D	3	A
	Pulse (Note 1)	I_{DP}	9	A
Drain power dissipation ($T_c = 25^\circ C$)		P_D	100	W
Single pulse avalanche energy (Note 2)		E_{AS}	295	mJ
Avalanche current		I_{AR}	3	A
Repetitive avalanche energy (Note 3)		E_{AR}	10.0	mJ
Channel temperature		T_{ch}	150	$^\circ C$
Storage temperature range		T_{stg}	-55~150	$^\circ C$



Weight: 2.0 g (typ.)

Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th(ch-c)}$	1.25	$^\circ C / W$
Thermal resistance, channel to ambient	$R_{th(ch-a)}$	83.3	$^\circ C / W$

Note 1: Please use devices on condition that the channel temperature is below $150^\circ C$.

Note 2: $V_{DD} = 90 V, T_{ch} = 25^\circ C$ (initial), $L = 60.0 mH, R_G = 25 \Omega, I_{AR} = 3 A$

Note 3: Repetitive rating: Pulse width limited by maximum channel temperature

This transistor is an electrostatic sensitive device.

Please handle with caution.

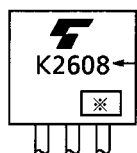
Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	$V_{GS} = \pm 30\text{ V}, V_{DS} = 0\text{ V}$	—	—	± 10	μA
Gate-source breakdown voltage		$V_{(BR)GSS}$	$I_G = \pm 10\ \mu\text{A}, V_{DS} = 0\text{ V}$	± 30	—	—	V
Drain cut-off current		I_{DSS}	$V_{DS} = 720\text{ V}, V_{GS} = 0\text{ V}$	—	—	100	μA
Drain-source breakdown voltage		$V_{(BR)DSS}$	$I_D = 10\text{ mA}, V_{GS} = 0\text{ V}$	900	—	—	V
Gate threshold voltage		V_{th}	$V_{DS} = 10\text{ V}, I_D = 1\text{ mA}$	2.0	—	4.0	V
Drain-source ON resistance		$R_{DS(ON)}$	$V_{GS} = 10\text{ V}, I_D = 1.5\text{ A}$	—	3.73	4.3	Ω
Forward transfer admittance		$ Y_{fs} $	$V_{DS} = 20\text{ V}, I_D = 1.5\text{ A}$	0.65	2.6	—	S
Input capacitance		C_{iss}	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	—	750	—	pF
Reverse transfer capacitance		C_{rss}		—	10	—	
Output capacitance		C_{oss}		—	70	—	
Switching time	Rise time	t_r		—	15	—	ns
	Turn-on time	t_{on}		—	55	—	
	Fall time	t_f		—	30	—	
	Turn-off time	t_{off}		—	110	—	
Total gate charge (gate-source plus gate-drain)		Q_g	$V_{DD} \approx 400\text{ V}, V_{GS} = 10\text{ V}, I_D = 3\text{ A}$	—	25	—	nC
Gate-source charge		Q_{gs}		—	13	—	
Gate-drain ("miller") Charge		Q_{gd}		—	12	—	

Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	3	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	9	A
Forward voltage (diode)	V_{DSF}	$I_{DR} = 3\text{ A}, V_{GS} = 0\text{ V}$	—	—	-1.9	V
Reverse recovery time	t_{rr}	$I_{DR} = 3\text{ A}, V_{GS} = 0\text{ V}, dI_{DR} / dt = 100\text{ A} / \mu\text{s}$	—	1200	—	ns
Reverse recovery charge	Q_{rr}		—	8.5	—	μC

Marking

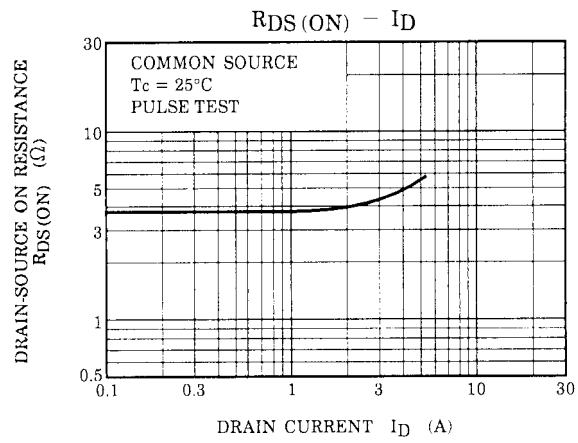
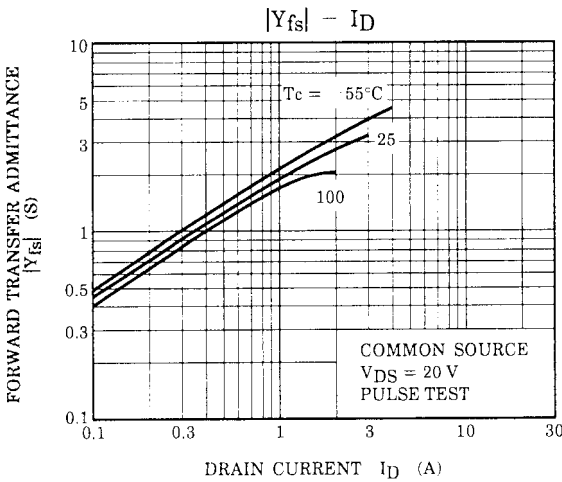
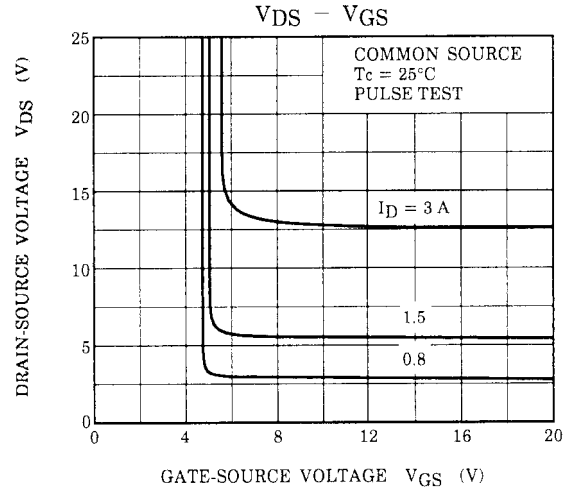
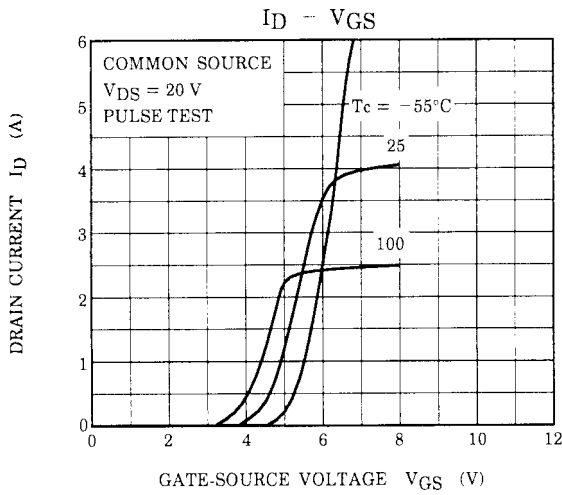
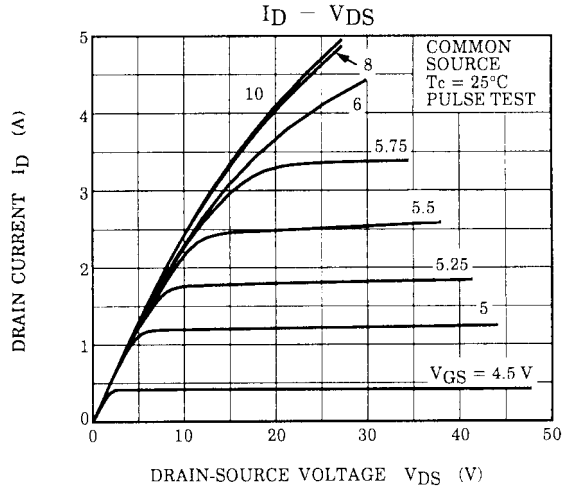
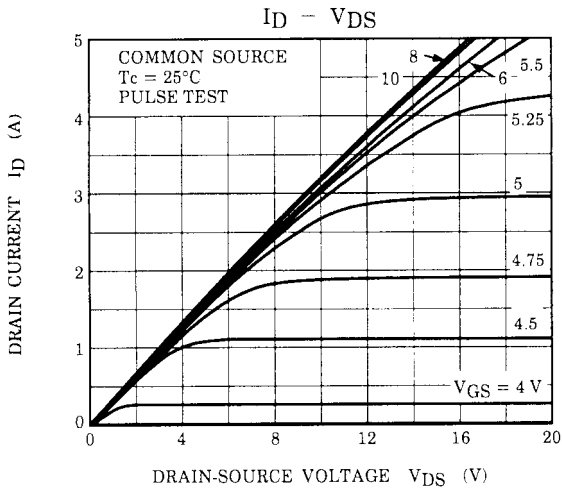


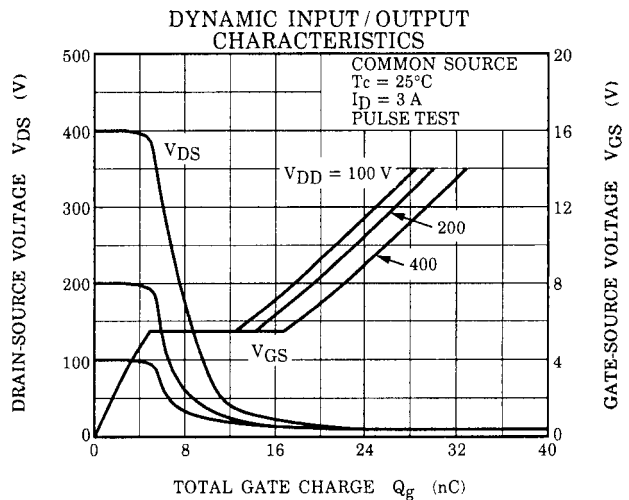
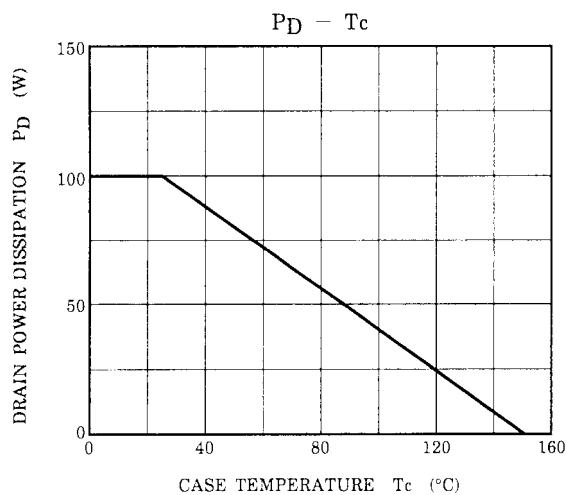
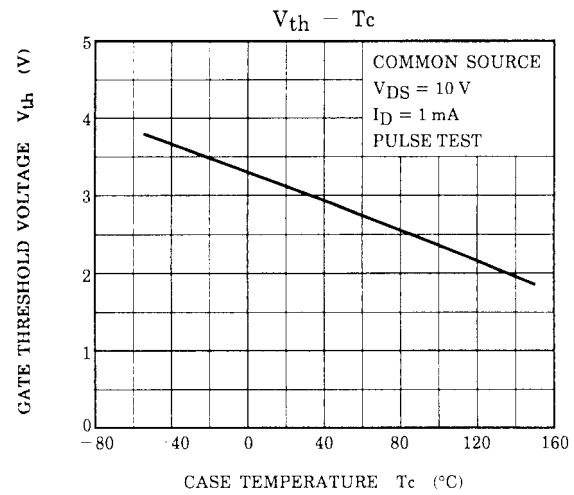
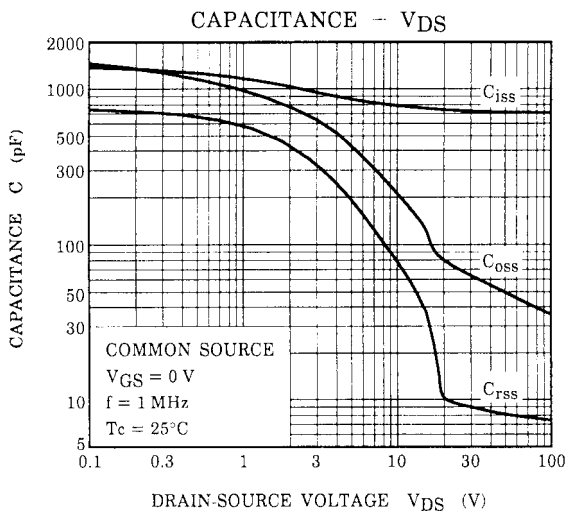
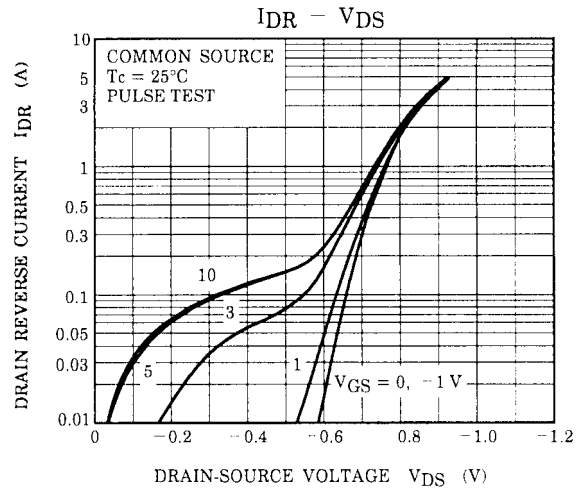
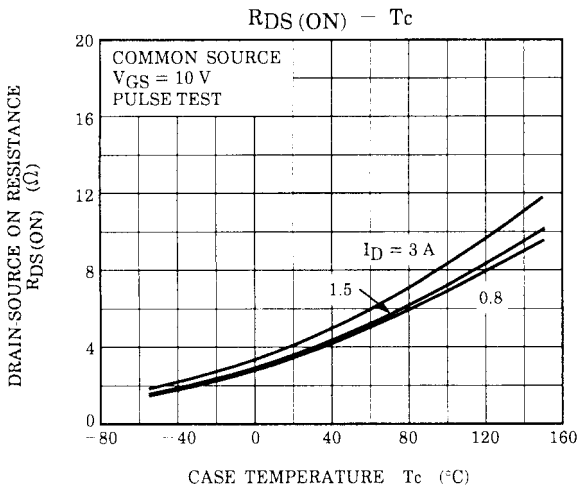
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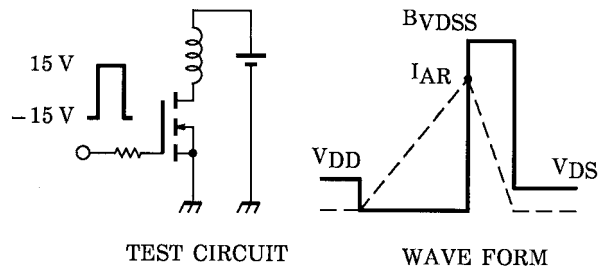
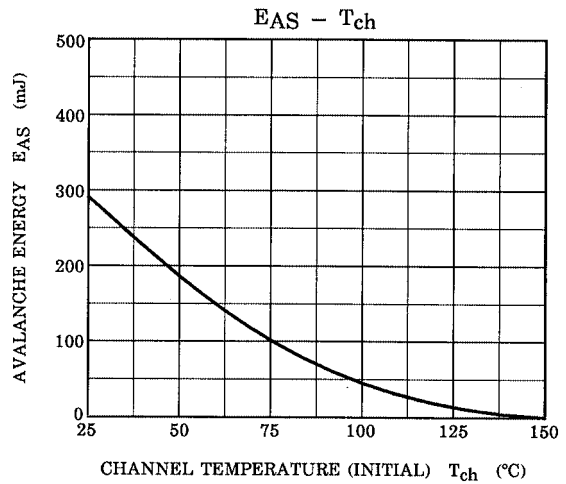
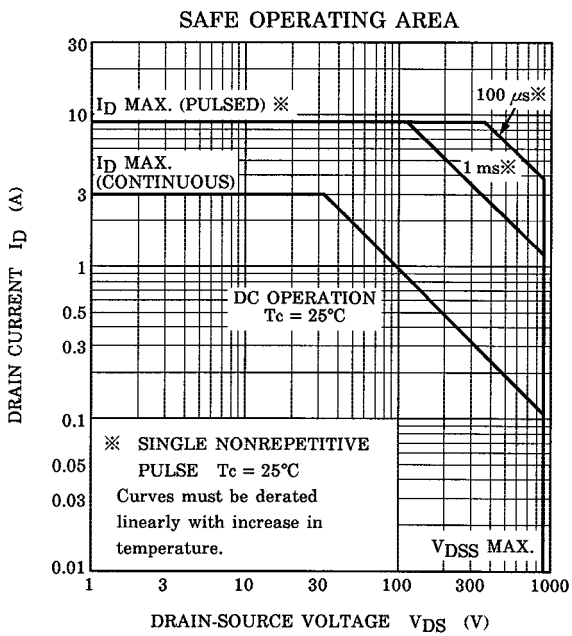
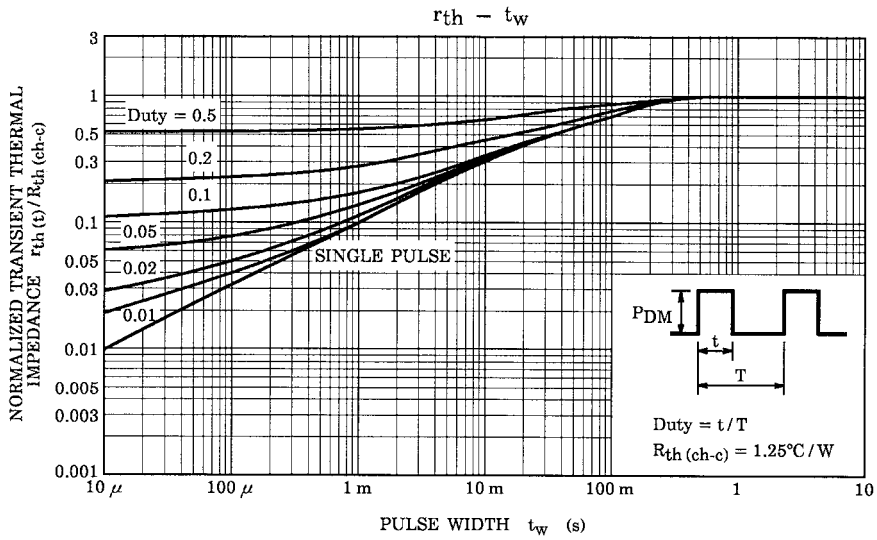
※ Lot Number

□ □ — Month (Starting from Alphabet A)

□ — Year (Last Number of the Christian Era)







$$R_G = 25 \Omega$$

$$V_{DD} = 90 \text{ V}, L = 60 \text{ mH} \quad EAS = \frac{1}{2} \cdot L \cdot I_{AR}^2 \cdot \left(\frac{BVDSS}{BVDSS - V_{DD}} \right)$$

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