



LA4282

2-Channel 10 W AF Power Amplifier for Use in Home Stereo, TV Applications

Overview

The LA4282 is an IC which seals a high-output power amplifier for TVs and monitors in a compact package.

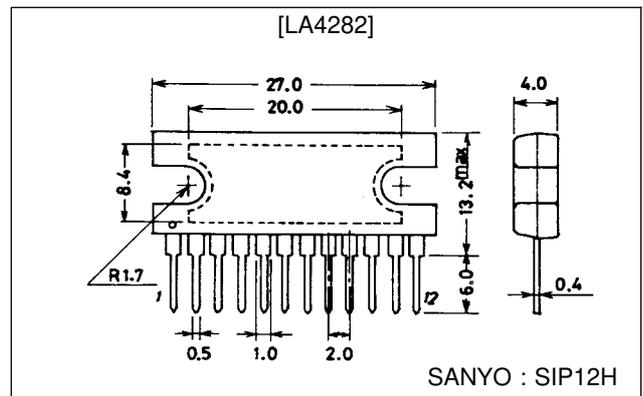
Features

- High-power 2-channel AF power amplifier
- Low distortion
- Minimum number of external parts required (no bootstrap capacitor required)
- Low pop noise at the time of power supply ON/OFF
- Good ripple rejection (58 dB typ)
- Wide operating voltage range
- External muting available
- On-chip protector against abnormality (thermal shutdown, overvoltage)

Package Dimensions

unit : mm

3049A-SIP12H



Specifications

Maximum Ratings at Ta = 25 °C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC \text{ max}}$	Quiescent	45	V
Maximum output current	$I_{O \text{ peak}}$		4	A
Allowable power dissipation	$P_d \text{ max}$	With heat sink	25	W
Operating temperature	T_{opr}		-20 to +75	°C
Storage temperature	T_{stg}		-40 to +150	°C

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		32	V
	$V_{CC \text{ op}}$		10 to 40	V
Recommended load resistance	R_L		8	Ω

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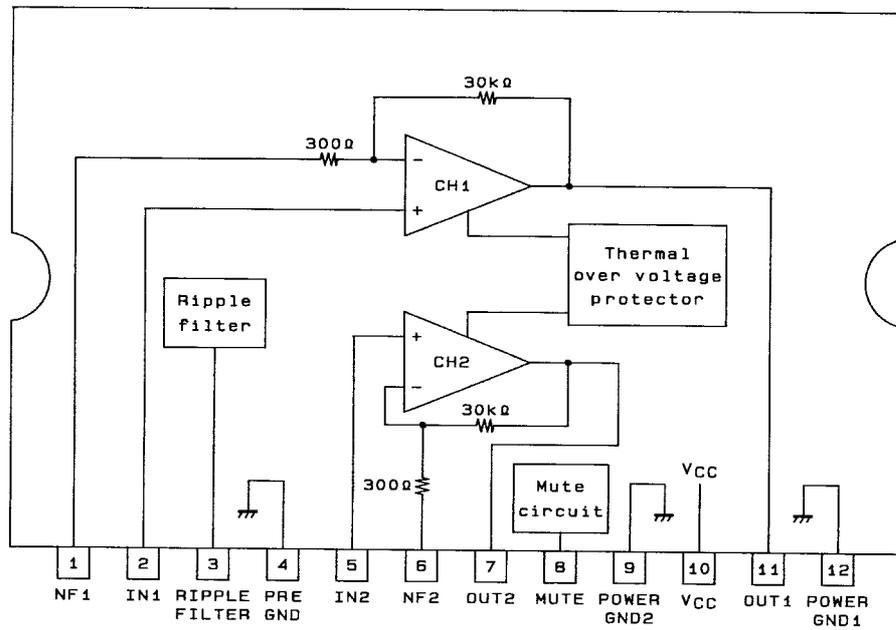
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**Operating Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC} = 32\text{ V}$, $R_L = 8\ \Omega$, $f = 1\text{ kHz}$, $R_g = 600\ \Omega$,
See Test Circuit.**

Parameter	Symbol	Conditions	min	typ	max	Unit
Quiescent current	$I_{CCO(1)}$	Quiescent	30	60	100	mA
	$I_{CCO(2)}$	Muting switch On	30	56	100	mA
Voltage gain	VG		38	40	42	dB
Voltage gain difference	ΔVG				1.5	dB
Output power	$P_O(1)$	THD = 1%	9.0	10.0		W
	$P_O(2)$	THD = 3%	10.0	11.5		W
Total harmonic distortion	THD	$P_O = 2\text{ W}$		0.05	0.20	%
Output noise voltage	V_{NO}	$R_g = 10\text{ k}\Omega$, BW = 20 Hz to 20 kHz		0.25	1.0	mV
Ripple rejection	SVRR	$R_g = 10\text{ k}\Omega$, $f_R = 100\text{ Hz}$, $V_R = 0\text{ dBm}$	45	58		dB
Crosstalk	CT	$R_g = 10\text{ k}\Omega$	45	60		dB
Muting	$V_{O(MT)}$	Muting switch On, $V_{IN} = -5\text{ dBm}$			-35	dBm

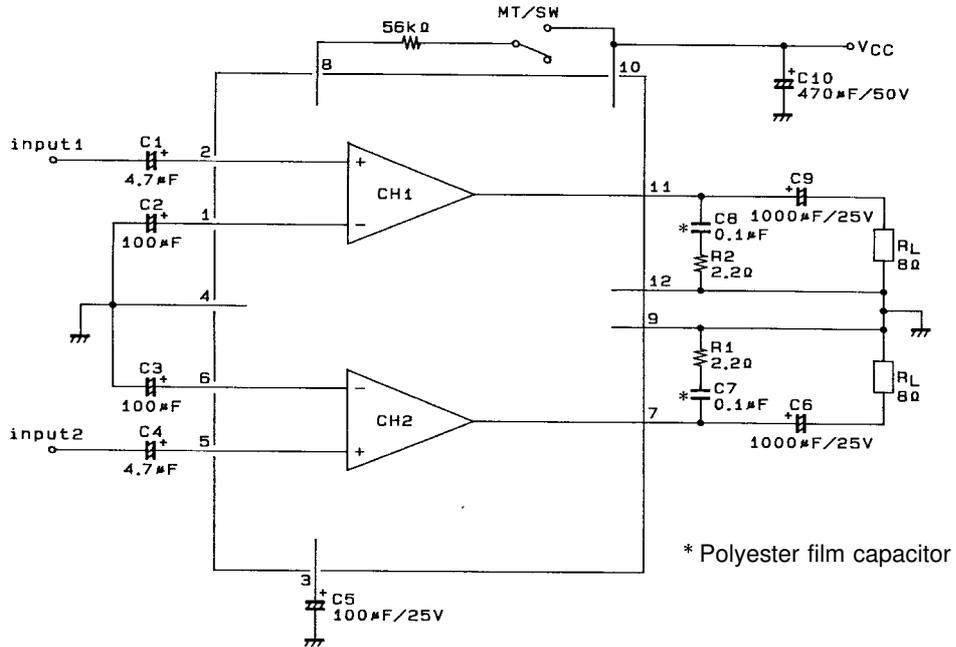
Equivalent Circuit Block Diagram and Pin Assignment



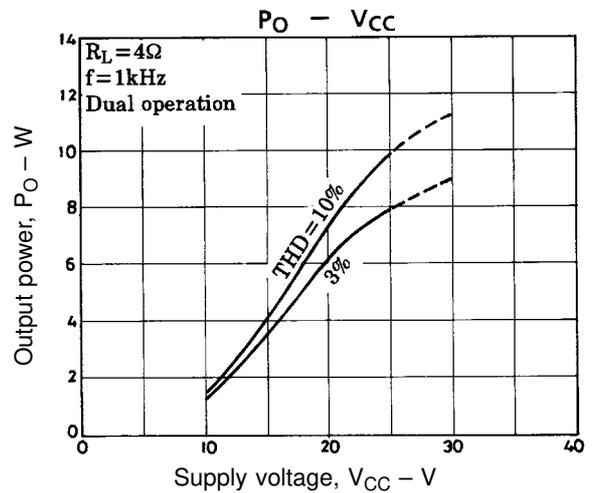
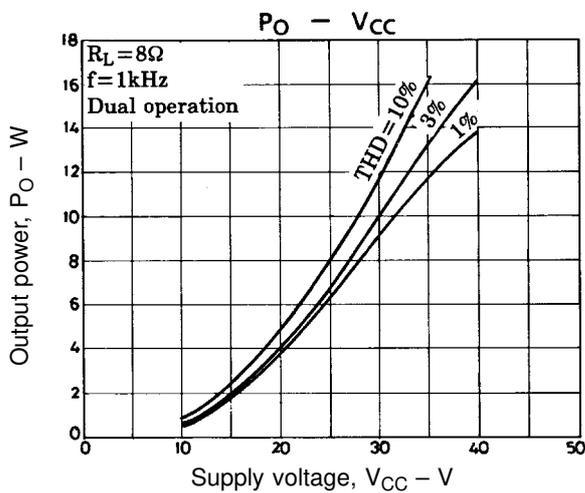
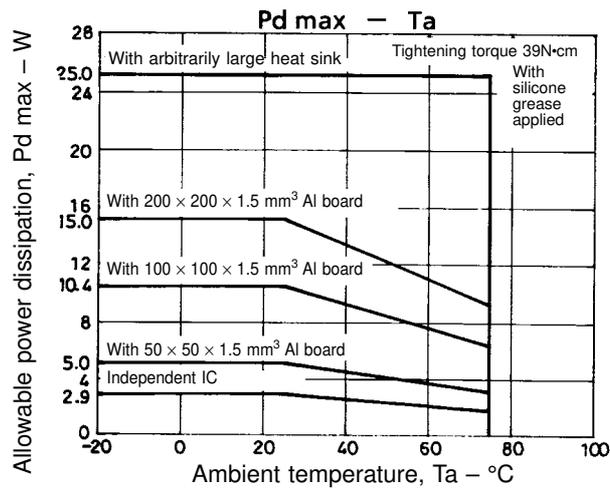
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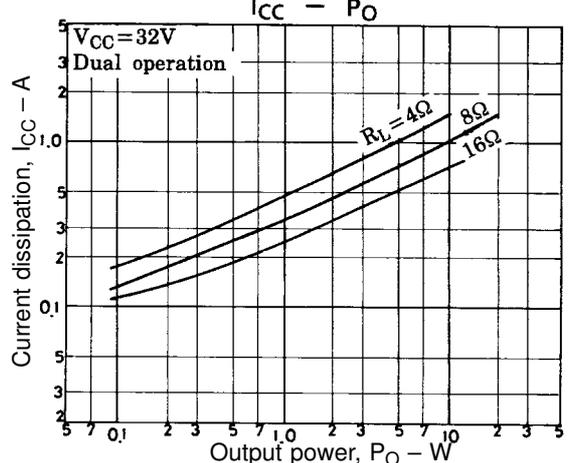
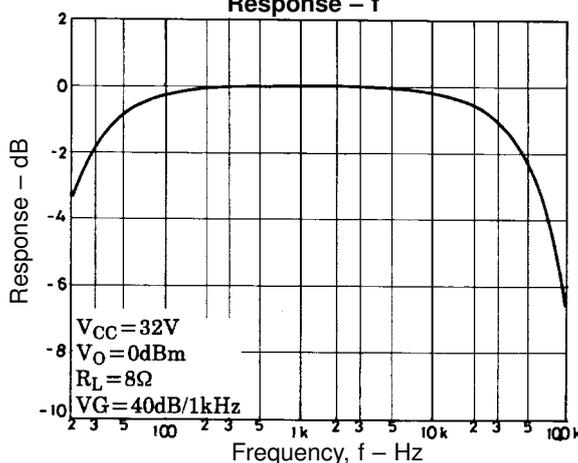
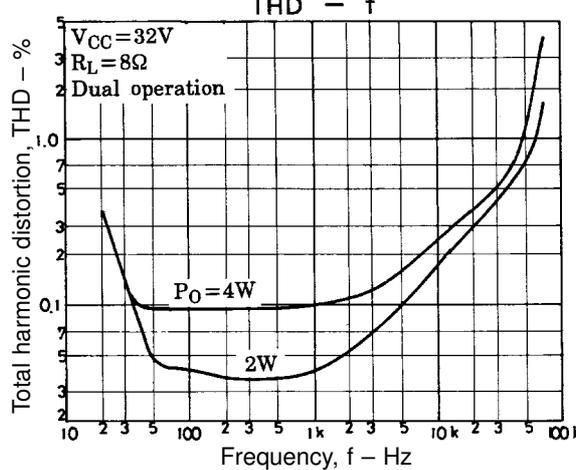
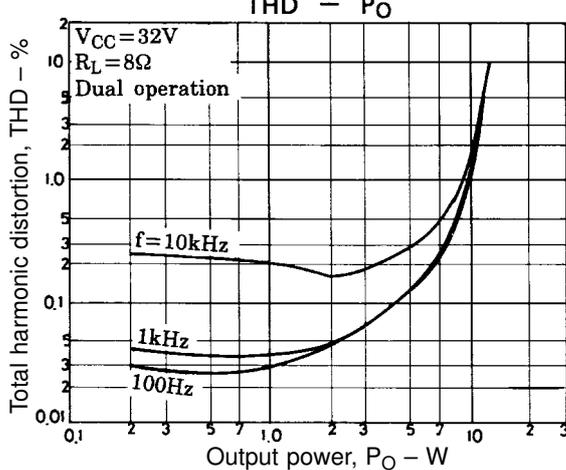
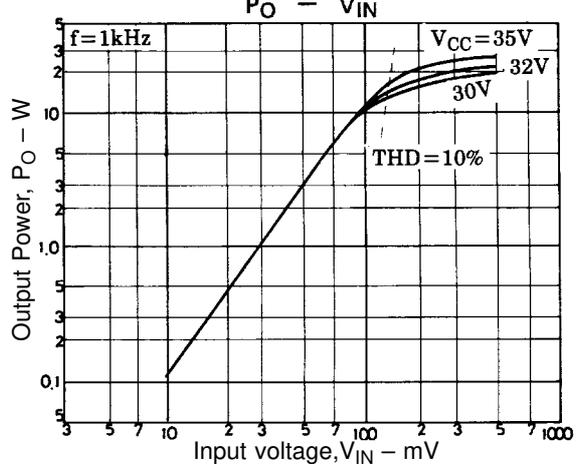
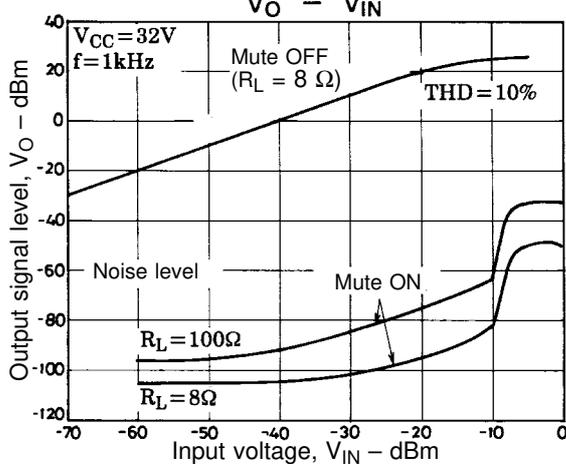
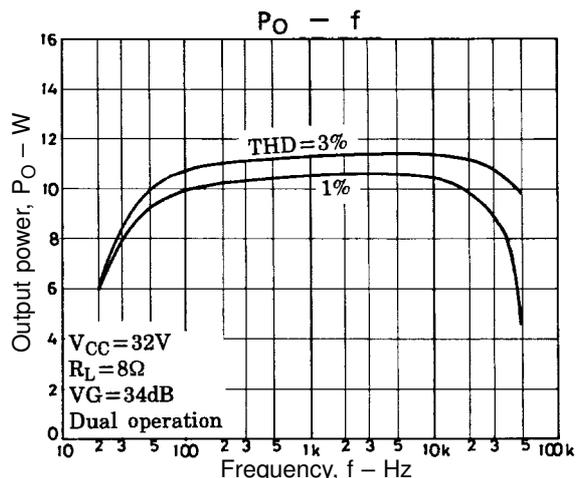
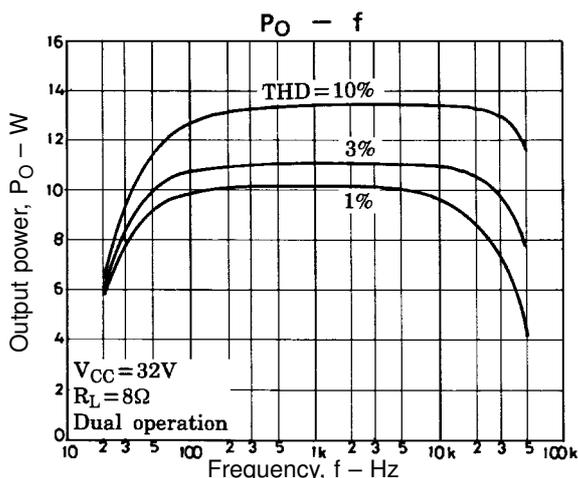
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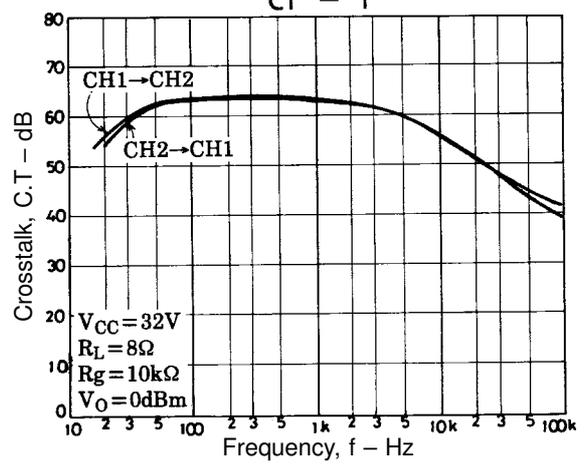
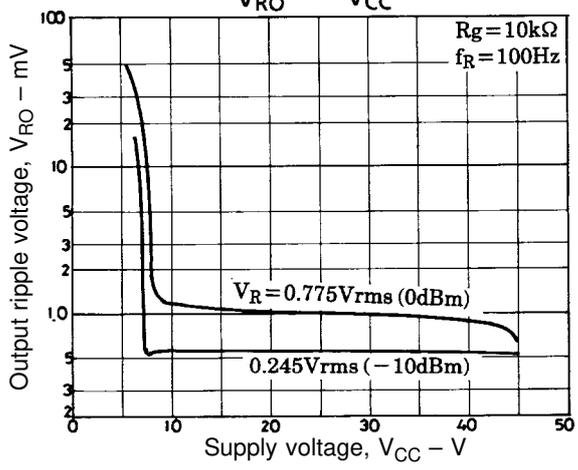
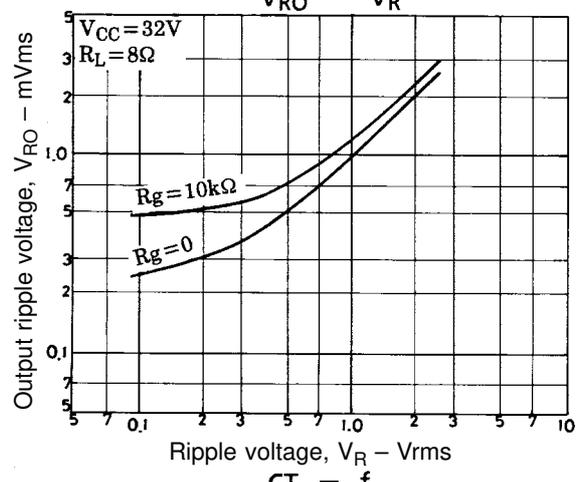
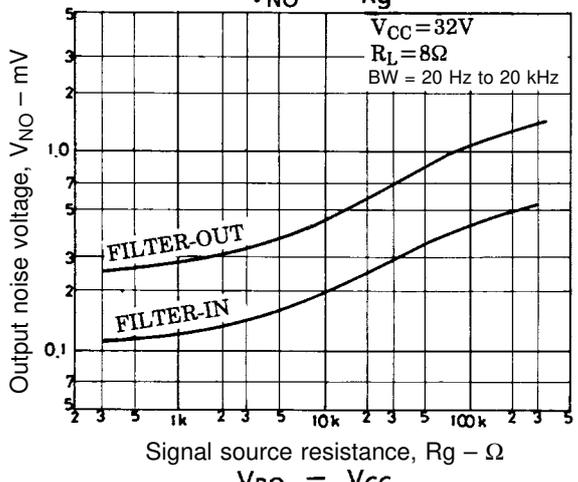
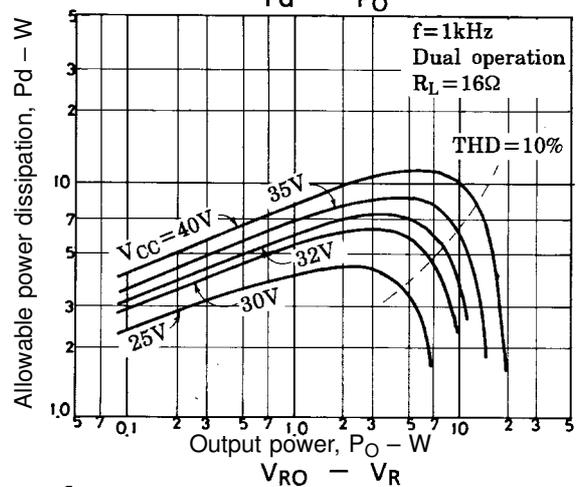
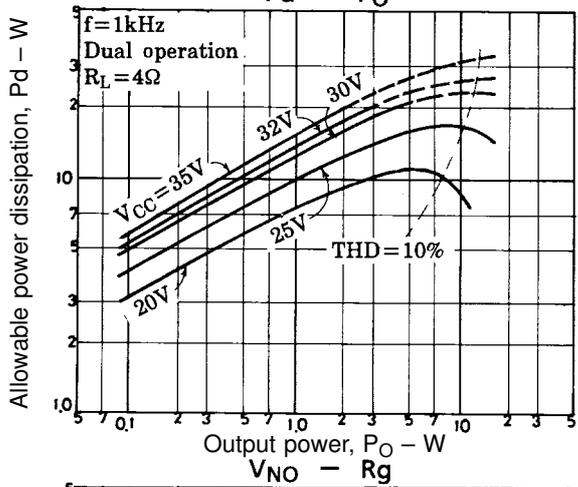
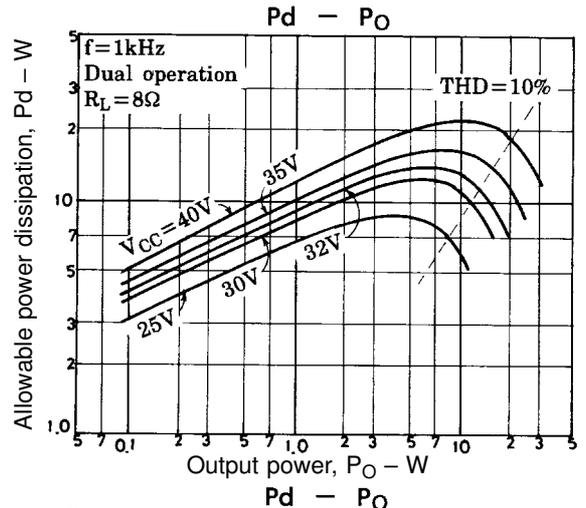
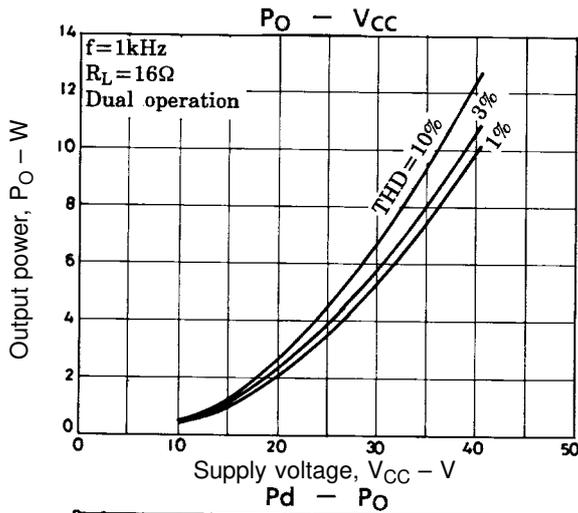
Test Circuit



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