

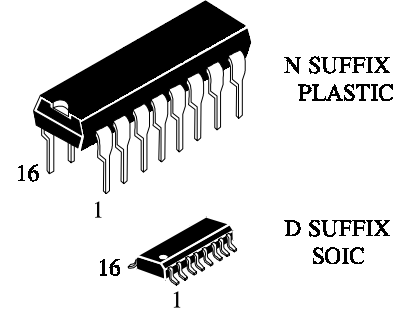
IW4520B

Dual Up-Counter
High-Voltage Silicon-Gate CMOS

The IW4520B Dual Binary Up-Counter consists two identical, internally synchronous 4-stage counters. The counter stages are D-type flip-flops having interchangeable CLOCK and ENABLE lines for incrementing on either the positive-going or negative-going transition. For single-unit operation the ENABLE input is maintained high and the counter advances on each positive-going transition of the CLOCK. The counters are cleared by high levels on their RESET lines.

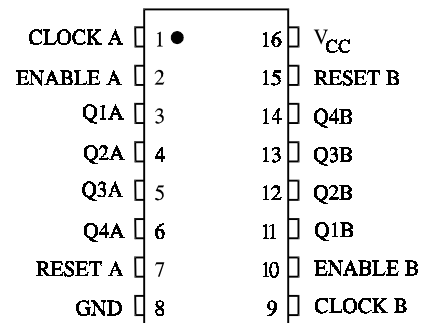
The counter can be cascaded in the ripple mode by connecting Q4 to the enable input of the subsequent counter while the CLOCK input of the latter is held low.

- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
 - 1.0 V min @ 5.0 V supply
 - 2.0 V min @ 10.0 V supply
 - 2.5 V min @ 15.0 V supply

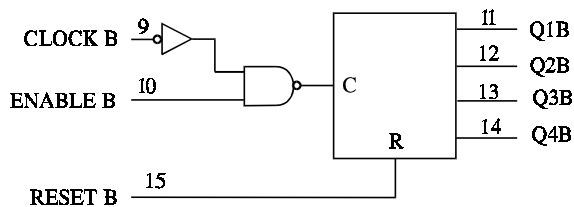
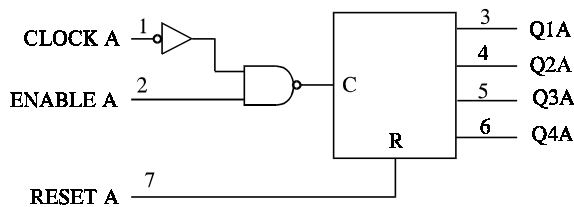


ORDERING INFORMATION
 IW4520BN Plastic
 IW4520BD SOIC
 $T_A = -55^\circ$ to 125° C for all packages

PIN ASSIGNMENT



LOGIC DIAGRAM



PIN 16=V_{CC}
 PIN 8=GND

FUNCTION TABLE

Inputs			Outputs
CLOCK	ENABLE	RESET	Mode
	H	L	Increment Counter
L		L	Increment Counter
	X	L	No Change
X		L	No Change
	L	L	No Change
H		L	No Change
X	X	H	Q1 thru Q4=L

X = don't care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V _{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
V _{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{IN}	DC Input Current, per Pin	±10	mA
P _D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
P _D	Power Dissipation per Output Transistor	100	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	3.0	18	V
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).
Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				≥-55°C	25°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} = 0.5 V or V _{CC} - 0.5V	5.0	3.5	3.5	3.5	V
		V _{OUT} = 1.0 V or V _{CC} - 1.0 V	10	7	7	7	
		V _{OUT} = 1.5 V or V _{CC} - 1.5V	15	11	11	11	
V _{IL}	Maximum Low -Level Input Voltage	V _{OUT} = 0.5 V or V _{CC} - 0.5V	5.0	1.5	1.5	1.5	V
		V _{OUT} = 1.0 V or V _{CC} - 1.0 V	10	3	3	3	
		V _{OUT} = 1.5 V or V _{CC} - 1.5V	15	4	4	4	
V _{OH}	Minimum High-Level Output Voltage	V _{IN} =GND or V _{CC}	5.0	4.95	4.95	4.95	V
			10	9.95	9.95	9.95	
			15	14.95	14.95	14.95	
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} =GND or V _{CC}	5.0	0.05	0.05	0.05	V
			10	0.05	0.05	0.05	
			15	0.05	0.05	0.05	
I _{IN}	Maximum Input Leakage Current	V _{IN} = GND or V _{CC}	18	±0.1	±0.1	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} = GND or V _{CC}	5.0	5	5	150	μA
			10	10	10	300	
			15	20	20	600	
			20	100	100	3000	
I _{OL}	Minimum Output Low (Sink) Current	V _{IN} = GND or V _{CC} U _{OL} =0.4 V U _{OL} =0.5 V U _{OL} =1.5 V	5.0	0.64	0.51	0.36	mA
			10	1.6	1.3	0.9	
			15	4.2	3.4	2.4	
I _{OH}	Minimum Output High (Source) Current	V _{IN} = GND or V _{CC} U _{OH} =2.5 V U _{OH} =4.6 V U _{OH} =9.5 V U _{OH} =13.5 V	5.0	-2	-1.6	-1.15	mA
			5.0	-0.64	-0.51	-0.36	
			10	-1.6	-1.3	-0.9	
			15	-4.2	-3.4	-2.4	

AC ELECTRICAL CHARACTERISTICS($C_L=50\text{pF}$, $R_L=200\text{k}\Omega$, Input $t_r=t_f=20\text{ ns}$)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			≥-55°C	25°C	≤125°C	
f _{max}	Maximum Clock Frequency, (Figure 1)	5.0 10 15	1.5 3 4	1.5 3 4	0.75 1.5 2	MHz
t _{PHL} , t _{PLH}	Maximum Propagation Delay, Clock or Enable to Output (Figures 1,3)	5.0 10 15	560 230 160	560 230 160	1120 460 320	ns
t _{PHL}	Maximum Propagation Delay, Reset to Output (Figure 2)	5.0 10 15	650 225 170	650 225 170	1300 450 340	ns
t _{THL} , t _{TLH}	Maximum Output Transition Time, Any Output (Figure 1)	5.0 10 15	200 100 80	200 100 80	400 200 160	ns
C _{IN}	Maximum Input Capacitance	-		7.5		pF

TIMING REQUIREMENTS($C_L=50\text{pF}$, $R_L=200\text{ k}\Omega$, Input $t_r=t_f=20\text{ ns}$)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			≥-55°C	25°C	≤125°C	
t _w	Minimum Pulse Width, Clock (Figure 1)	5.0 10 15	200 100 70	200 100 70	400 200 140	ns
t _w	Minimum Pulse Width, Reset (Figure 2)	5.0 10 15	250 110 80	250 110 80	500 220 160	ns
t _w	Minimum Pulse Width, Enable (Figure 3)	5.0 10 15	400 200 140	400 200 140	800 400 280	ns
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	5.0 10 15	15 5 5	15 5 5	15 5 5	μs

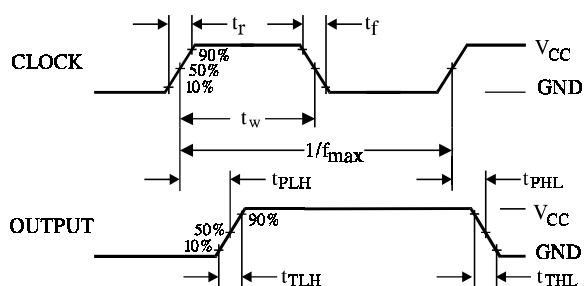


Figure 1. Switching Waveforms

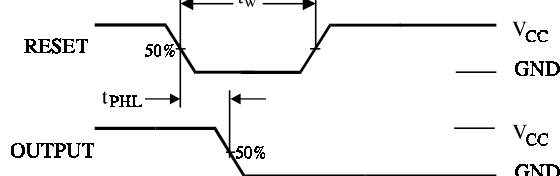


Figure 2. Switching Waveforms

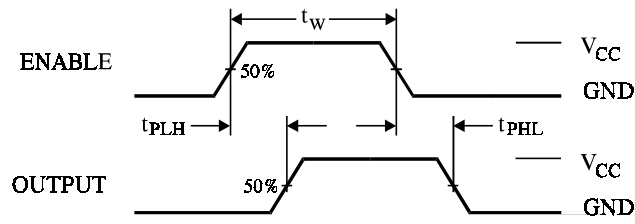
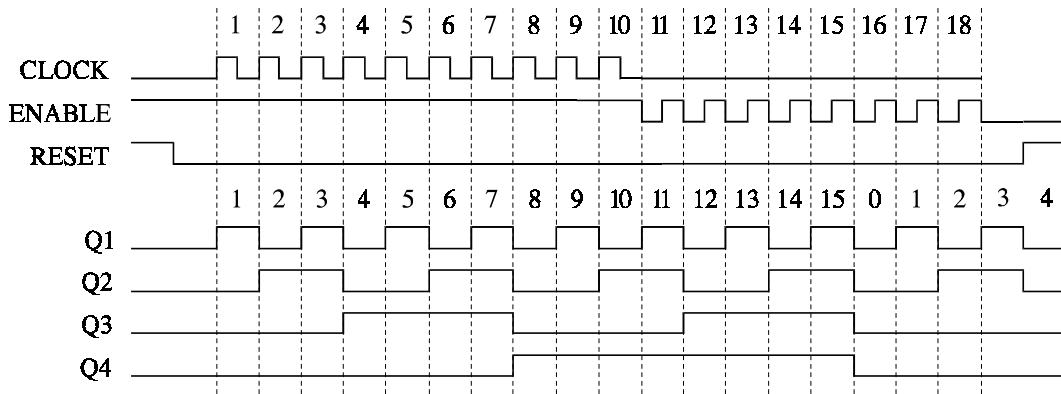


Figure 3. Switching Waveforms

TIMING DIAGRAM



**EXPANDED LOGIC DIAGRAM
(1/2 of the Device)**

