SSI 78A093A/B
CMOS 12x8x1 Crosspoint Switch With Control Memory

July 1990

DESCRIPTION

The SSI 78A093 is a 12x8 matrix-array crosspoint-switching IC for telecom-switching and industrial control-routing applications. Standard integrated features include microprocessor-control inputs, line decoder, address latches, and 6 Vp-p analog-signal capability. The product is available with two different power supply configurations: The SSI 78A093A accepts power through the VSS and VDD pins; the SSI 78A093B has an altered pin-out and offers a separate logic ground pin. Both versions offer excellent crosstalk immunity, low feedthrough (–95dB at 1KHz), extra-high isolation between any two switches connected to X0 channel, and less than 1% total distortion at 0 dBm. The X0 channel is optimized for "ON HOLD" use by providing high isolation between switches connected to X0. The SSI 78A093 employs CMOS design technology for low-power operation. Power requirement for both the A and B versions of the SSI 78A093 is 5 to 16 volts. Both versions are packaged in a standard 40-pin plastic DIP or 44-pin PLCC.

FEATURES

- 96 crosspoint switches in a 12x8 array
- µP-compatible control inputs
- On-chip line demultiplexer
- Low ON resistance: 28 ohms at VDD = 12V typical
- 5 to 16-volt supply operating range
- 6 Vp-p analog signal capability
- Address latches on-chip
- Optimized performance on X0 channel
- Less than 1% total distortion at 0 dBm
- -95 dB feedthrough at 1kHz
- Extra-low crosstalk between any two switches connected to X0
- 78A093B version offers separate logic ground for flexible system design
- Low-power CMOS design
- TTL or CMOS-compatible inputs
- 40-pin plastic DIP or 44-pin PLCC

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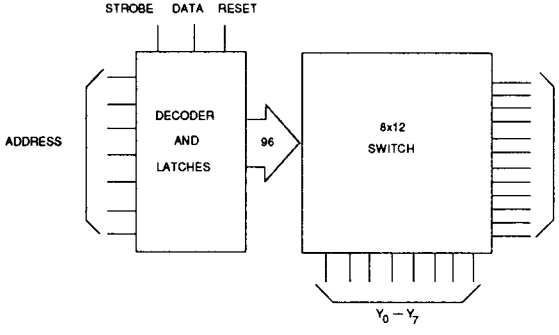
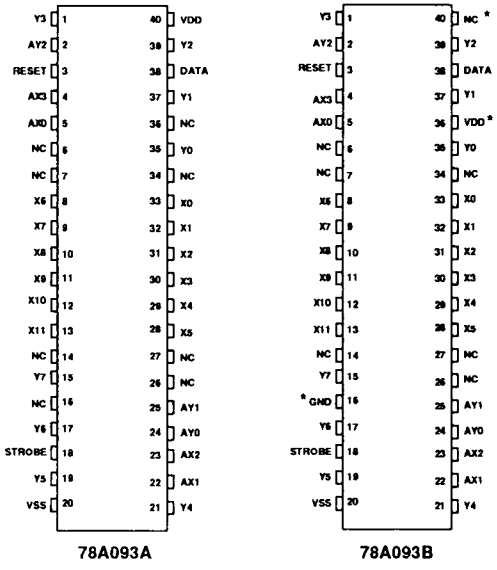
BLOCK DIAGRAM



PIN DIAGRAM



* different pins relative to 78A093A

NOTE: Please see last page for PLCC pinout.

CAUTION: Use handling procedures necessary for a static sensitive component.

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CMOS 12x8x1
Crosspoint Switch
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FUNCTIONAL DESCRIPTION

A functional block diagram of the device is presented in Figure 1. The IC contains a 12x8 matrix of analog switches, each with a latch to maintain its on (closed) or off (open) state. Seven ADDRESS lines, AX0-AX3 and AY0-AY2, are provided to address any one of the 96 switches. The DATA line may be held high to turn the switch on, or low to turn it off. The state of the ADDRESS and DATA lines can be set concurrently or separately. Finally, a positive pulse to the STROBE line initiates the action determined by the ADDRESS and DATA lines. All 96 switches may be turned off by forcing the RESET line high. All control lines (ADDRESS, DATA, STROBE, and RESET) are level sensitive.

The IC has two power supply configurations: the A-version has VDD and VSS power supply pins; the B-version has VDD, VSS and a GND pin. The GND pin is provided as a reference voltage for digital inputs. For proper operation, the positive supply must be at least 4.5 volts above GND.

The switches are designed to provide low resistance connections when turned on. Any Y switches connecting to the X0 channel are optimized to provide lower ON resistance. Furthermore, the X0 channel switches, when turned on, provide maximized isolation between the Y channels when X0 is grounded or connected to a low impedance source.

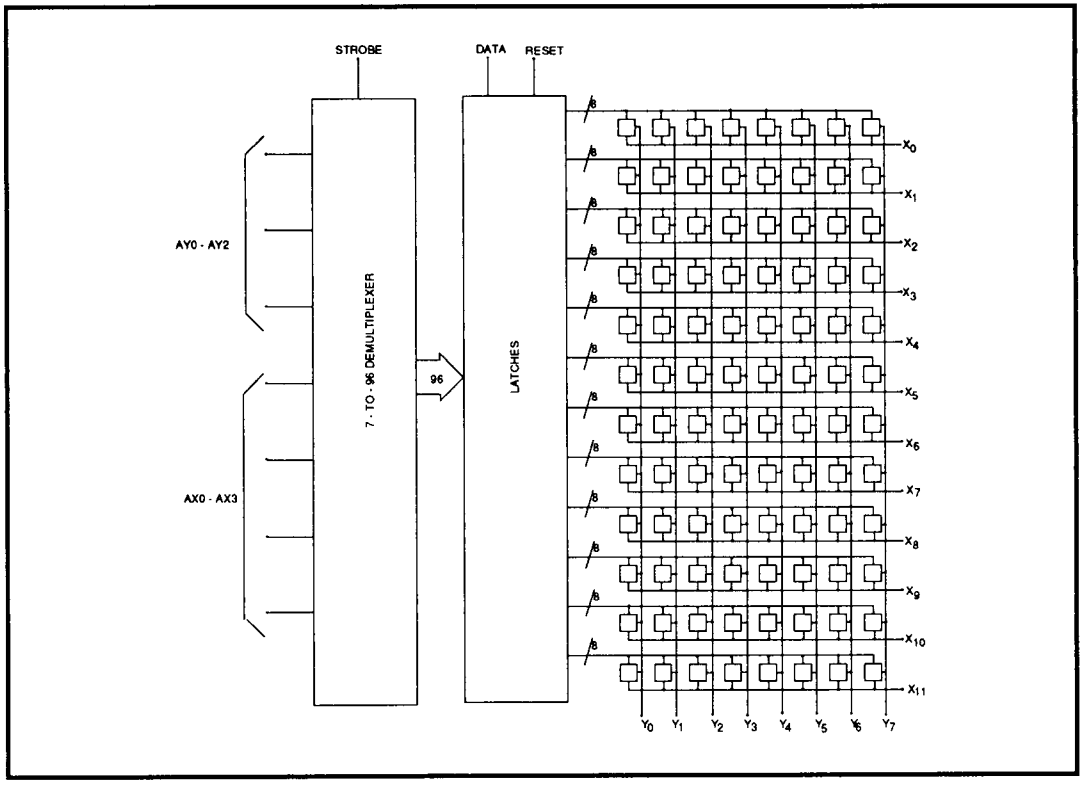


FIGURE: 1

PIN DESCRIPTION

NAME	A-PIN # (DIP)	B-PIN # (DIP)	TYPE	DESCRIPTION
POWER				
VDD	40	36	I	Positive power supply.
VSS	20	20	I	Negative power supply.
GND	-	16	I	Digital signal ground.
ADDRESS				
AX0-AX3	4, 5, 22, 23		I	X address lines. These 4 pins are used to select one of the 12 rows of switches. Refer to the truth table in figure 2, for legal addresses.
AY0-AY2	2, 24, 25		I	Y address lines. These 3 pins are used to select one of the 8 columns of switches. Refer to the truth table in figure 2, for legal addresses.
CONTROL				
DATA	38		I	This input determines if the selected switch will be turned on (closed) or off (opened). If the pin is held high, the selected switch will be closed. If the pin is held low, the switch will be opened.
STROBE	18		I	This pin enables whatever action is selected by the address and DATA pins. When the STROBE pin is held low, no switch openings or closing take place. When the STROBE pin is held high, the switch addressed by the select lines will be opened or closed (depending upon the state of the DATA pin).
RESET	3		I	Master Reset. This pin turns off (opens) all 96 switches. The states of the above control lines are irrelevant. This pin is active high.
DATA				
X0-X11	8-13, 28-33		I/O	Analog Input/Outputs. These pins are connected to the rows of the switch matrix.
Y0-Y7	1, 15, 17, 19, 21, 35, 37, 39		I/O	Analog Input/Outputs. These pins are connected to the columns of the switch matrix.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device or affect device reliability.

PARAMETER	RATING	UNIT
VDD with respect to VSS	-0.5 to 17.6	V
GND (B-Version only)	VSS -0.5 to VDD +0.5	V
Storage Temperature	-65 to 150	°C
Control Signals	GND -0.5 to VDD +0.5	V
Analog Signals	7	Vpp
Lead Temperature (soldering, 10 seconds)	300	°C

Address							Connections
AX0	AX1	AX2	AX3	AY0	AY1	AY2	
0	0	0	0	0	0	0	X0 - Y0
1	0	0	0	0	0	0	X1 - Y0
0	1	0	0	0	0	0	X2 - Y0
1	1	0	0	0	0	0	X3 - Y0
0	0	1	0	0	0	0	X4 - Y0
1	0	1	0	0	0	0	X5 - Y0
address not allowed 0	1	1	0	0	0	0	no connection
address not allowed 1	1	1	0	0	0	0	no connection
0	0	0	1	0	0	0	X6 - Y0
1	0	0	1	0	0	0	X7 - Y0
0	1	0	1	0	0	0	X8 - Y0
1	1	0	1	0	0	0	X9 - Y0
0	0	1	1	0	0	0	X10 - Y0
1	0	1	1	0	0	0	X11 - Y0
address not allowed 0	1	1	1	0	0	0	no connection
address not allowed 1	1	1	1	0	0	0	no connection
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	1 ↓ 1	0 ↓ 0	0 ↓ 0	X0 - Y1 ↓ ↓ X11- Y1
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	0 ↓ 0	1 ↓ 1	0 ↓ 0	X0 - Y2 ↓ ↓ X11- Y2
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	1 ↓ 1	1 ↓ 1	0 ↓ 0	X0 - Y3 ↓ ↓ X11- Y3
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	0 ↓ 0	0 ↓ 0	1 ↓ 1	X0 - Y4 ↓ ↓ X11- Y4
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	1 ↓ 1	0 ↓ 0	1 ↓ 1	X0 - Y5 ↓ ↓ X11- Y5
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	0 ↓ 0	1 ↓ 1	1 ↓ 1	X0 - Y6 ↓ ↓ X11- Y6
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	1 ↓ 1	1 ↓ 1	1 ↓ 1	X0 - Y7 ↓ ↓ X11- Y7

FIGURE 2: Truth Table

RECOMMENDED OPERATING CONDITIONS

The recommended operating conditions for the device are indicated in the table below. Performance specifications do not apply when the device is operated outside these limits.

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNIT
VDD with respect to VSS		4.5		16.0	V
VDD with respect to GND		4.5		16.0	V
GND with respect to VSS		0		5.5	V
Analog Input Voltages VIN				6	Vpp
Analog Currents				10	mA
Ambient Temperature		0		85	°C

D.C. CHARACTERISTICS

TA = 25°C, VSS = 0V, GND = 0, VDD = 13.2V, RL = 1K, CL = 50pF, UNLESS OTHERWISE NOTED.
Positive current is defined as flowing into the device.

PARAMETERS		CONDITIONS	MIN	NOM	MAX	UNIT
Supply Current IDD				14	20	mA
CROSSPOINT						
ON resistance	X0 channel (X0-Yj)	VIN ≤ 6V		20		Ω
RON	other channels (Xi-Yj)	VIN ≤ 6V		28	45	Ω
ON resistance var.	X0 channel (X0-Yj)			5		Ω
Δ RON	other channels (Xi-Yj)			15	25	Ω
X capacitance	CX	(Switch off)			20	pF
Y capacitance	CY	(Switch off)			30	pF
CONTROL						
Input HIGH voltage	VIH	A-Version B-Version	2.0 GND +2.0			V V
Input LOW voltage	VIL	A-Version B-Version			0.8 GND +0.8	V V
Input leakage	IL		-0.1		0.1	µA

DYNAMIC CHARACTERISTICS AND TIMING

TA = 25°C, VDD = 13.2V, VSS = 0V, GND = 0V, RL = 1K, CL = 50 pF, UNLESS OTHERWISE NOTED. Digital input rise and fall times are 5nS. Output times are defined as the time to rise or fall from 0% to 10% of the full swing (see figure 3).

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNIT
CROSSPOINT					
Propagation Delay	1 Vpp sine wave @ 10 kHz		18	30	ns
Distortion	1 Vpp sine wave		0.2	1.0	%
Feedthrough	10 kHz, any switch off		-90	-80	dB
Yi to Yj isolation on X0 channel	Any two Y channels: Yi, Yj, X0-Yi, X0-Yj are on Xo grounded, Rin = 1K		-90	-60	dB
Crosstalk	1 kHz 1Vp-p sine wave 10 kHz		-97 -92		dB
CONTROL					
Delay: strobe to out TSZ			60	160	ns
Delay: address to out TAZ				200	ns
Delay: data to out TDZ				180	ns
Delay: reset to out TRZ			100	180	ns
Data setup time TSU			30		ns
Address setup time TAS			30		ns
Data hold time TH			30		ns
Address hold time TAH			30		ns
Strobe Pulse Width TST			50		ns
Reset Pulse Width TRST			50		ns

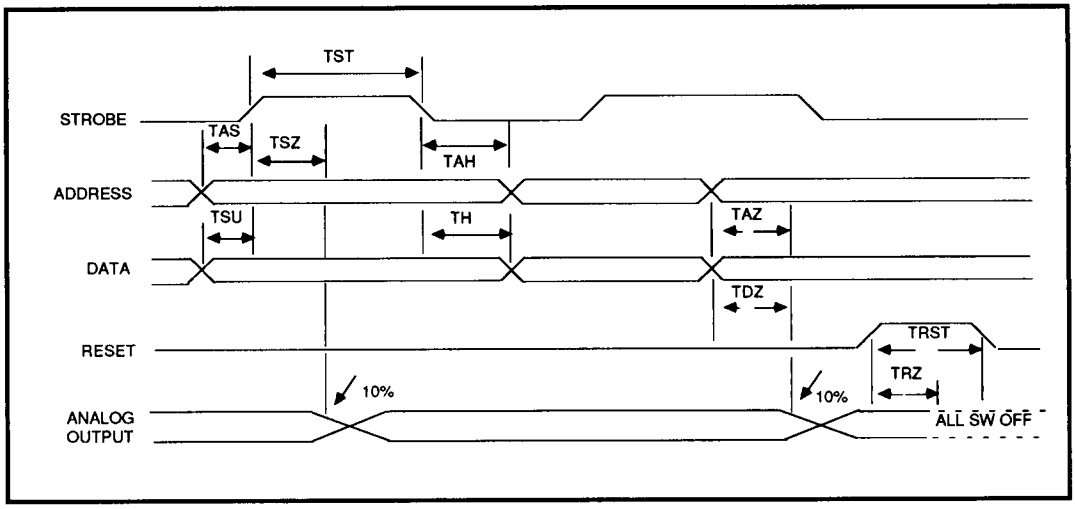


FIGURE 3: Timing Diagram

APPLICATIONS INFORMATION

Although the SSI 78A093 allows switching 96 possible signal paths, it is not limited to applications of only an 8x12x1 configuration. Figure 4 shows a method of addressing 4 separate 78A093's. In this example, the RESET, DATA, and ADDRESS lines are connected in parallel for the four devices. The logic for lines A, B and STROBE go to a 2-line to 4-line decoder with the STROBE used to both enable and clock the data. This decode (or a wider one) could be easily implemented with a single programmable logic device.

Figure 5 shows a case where both the X and Y lines have been expanded. This may be useful for applications where several different source/destination paths need to be controlled by a single controller. The A and B lines are decoded to select the desired device.

In Figure 6, the Y-lines of all devices are connected in parallel to allow an 8x48x1 switch configuration. The A and B inputs become in effect an extension of the X-address line. This could also be used to make a 32x12x1 matrix by tying the X-lines in parallel with the A and B inputs used as Y-address lines.

Figure 7 shows an application where switches in 2 devices are connected at the same time in a 12x8x2 matrix. This would be useful in applications requiring the switching of differential signals.

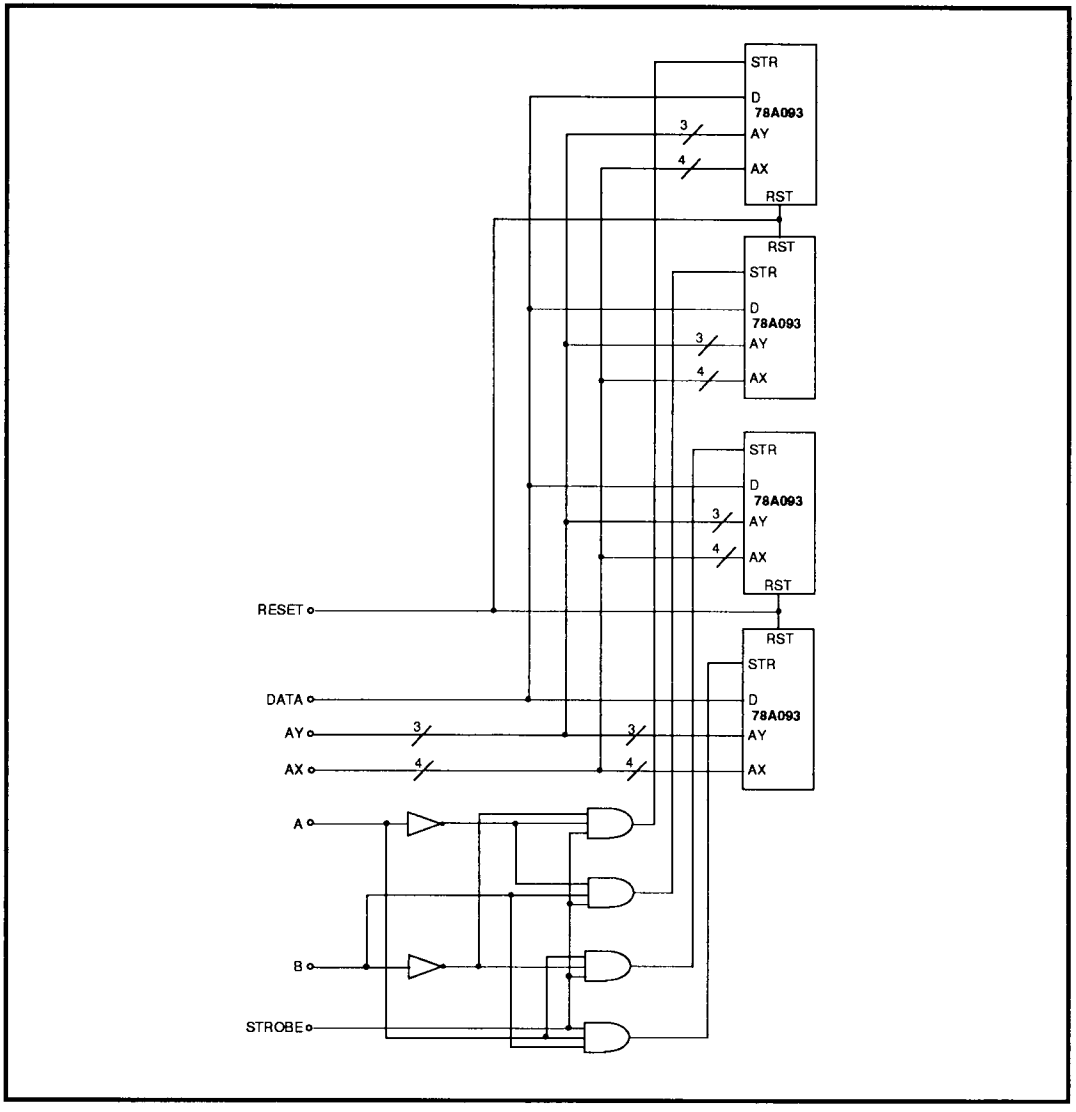


FIGURE 4

FIGURE 5

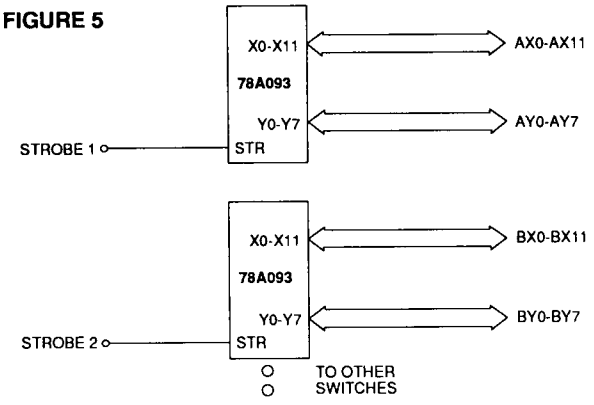


FIGURE 6

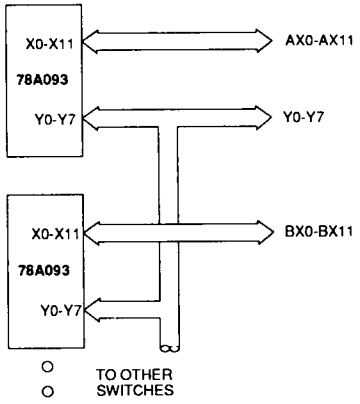
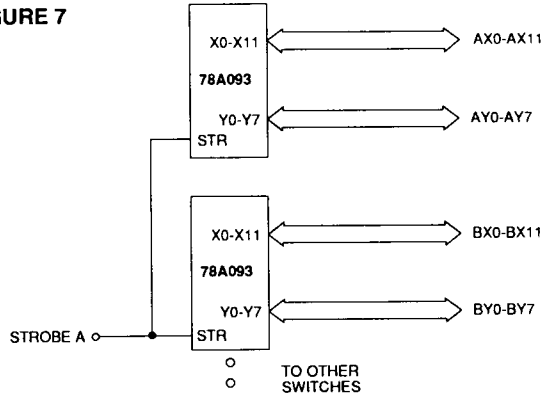


FIGURE 7



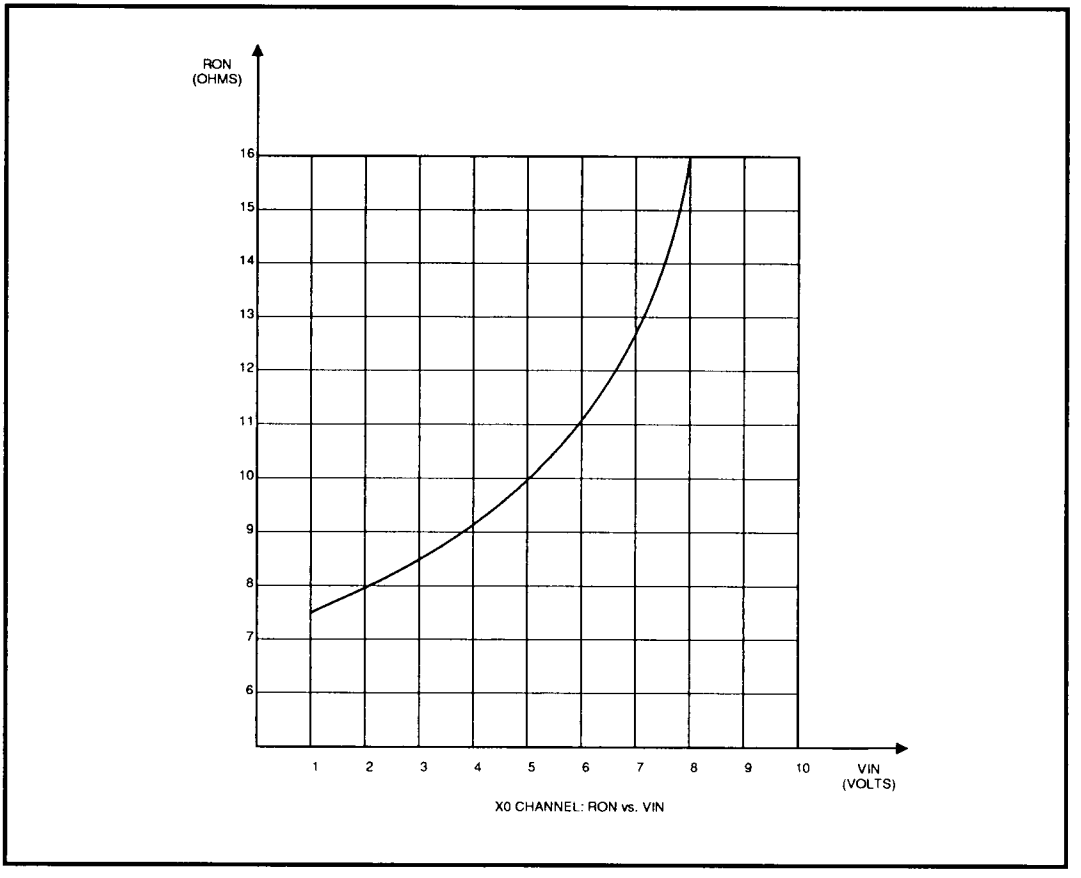


FIGURE 8: X0 - Channel: RON vs. VIN

Figure 8 is valid for all switches connected to the X0 channel only. The graph describes the behavior of the switch resistance RON as a function of the analog signal voltage VIN.

TEST CONDITIONS: VSS = 0V
VDD = 13.2V
RL = 1kΩ (Load Resistance)

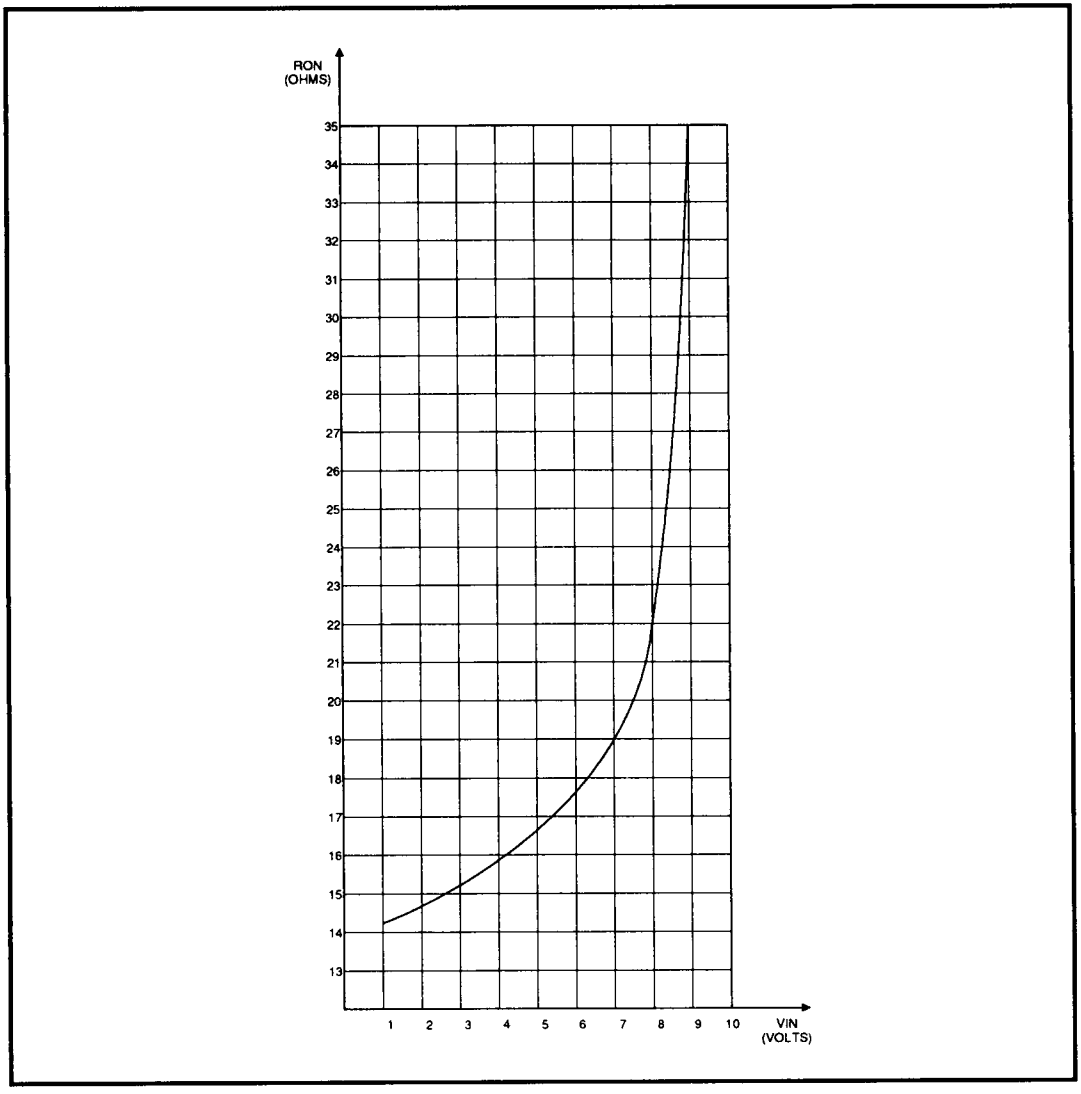


FIGURE 9: X1 - X11 Channel: RON vs. VIN

Figure 9 is valid for all switches connected to X1 thru X11 channels. The graph describes the behavior of the switch resistance RON as a function of the analog signal voltage VIN.

TEST CONDITIONS: VSS = 0V
VDD = 13.2V
RL = 1kΩ (Load Resistance)

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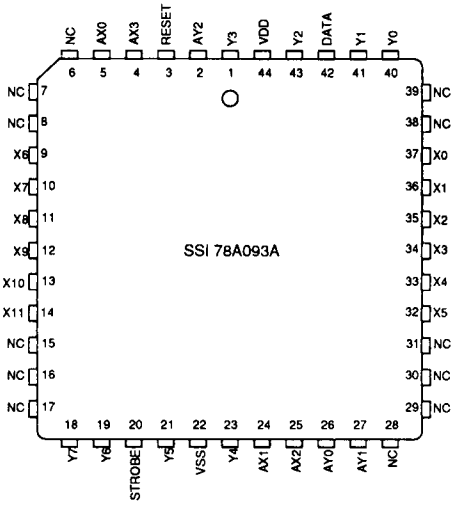
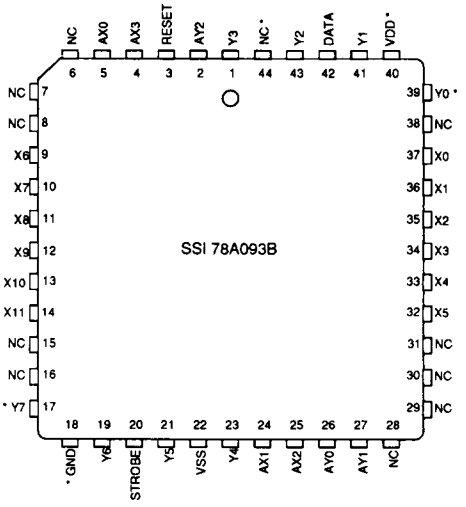
PACKAGE PIN DESIGNATIONS
(TOP VIEW)

Refer to the SSI Data Book for package dimensions.
Please see Page 1 for PDIP pinout.



44 - Pin PLCC
78A093A



44 - Pin PLCC
78A093B

* different pins relative to 78A093A

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 78A093, Version A		
Plastic Dual-In-Line	78A093A-CP	78A093A-CP
PLCC	78A093A-CH	78A093A-CH
SSI 78A093, Version B		
Plastic Dual-In-Line	78A093B-CP	78A093B-CP
PLCC	78A093B-CH	78A093B-CH

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