μPD8237A
HIGH-PERFORMANCE PROGRAMMABLE DMA CONTROLLER

Description

The μPD8237A high performance DMA controller is a peripheral interface circuit for microprocessor systems. It is designed to improve system performance by allowing external devices to directly transfer information to or from the system memory. Memory-to-memory transfer capability is also provided. The μPD8237A offers a wide variety of programmable control features to enhance data throughput and allow dynamic reconfiguration under program control.

The μPD8237A is designed to be used with an external 8-bit address register such as the 8282. It contains four independent channels and may be expanded to any number of channels by cascading additional controller chips.

The three basic transfer modes allow the user to program the types of DMA service. Each channel can be individually programmed to autoinitialize to its original condition following an end of process (EOP).

Each channel has a full 64K-byte address and word count capability.

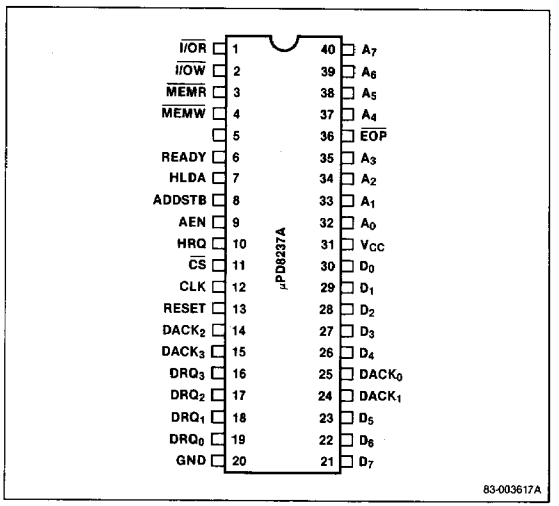
Features

- ☐ Memory-to-memory transfers
- ☐ Memory block initialization
- ☐ Address increment or decrement
- ☐ Four independent DMA channels
- ☐ Multiple transfer modes: block, demand, single word, cascade
- ☐ Independent autoinitialization of all channels
- ☐ Enable/disable control of individual DMA requests
- ☐ Independent polarity control of DREQ and DACK signals
- ☐ End of process input for terminating transfers
- ☐ Software DMA requests
- ☐ High performance: transfers up to 1.6 Mbs
- ☐ Directly expandable to any number of channels

Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPD8237AC-5	40-pin plastic DIP	5 MHz

Pin Configuration



Pin Identification

No.	Symbol	Function
1	$\overline{I/OR}$	I/O read control signal
2	$\overline{I/OW}$	I/O write control signal
3	$\overline{MEMR}$	Memory read output
4	$\overline{MEMW}$	Memory write output
5	—	Fixed, high level input
6	READY	Ready input
7	HLDA	Hold acknowledge input
8	ADDSTB	Address strobe output
9	AEN	Address enable output
10	HRQ	Hold request output
11	$\overline{CS}$	Chip select input
12	CLK	Clock input
13	RESET	Reset input
14, 15 24, 25	$DACK_2$, $DACK_3$ $DACK_1$, $DACK_0$	DMA acknowledge output
16-19	DRQ_3-DRQ_0	DMA request input
20	GND	Ground
21-23, 26-30	D_7-D_5 D_4-D_0	I/O data bus
31	V_{CC}	Power supply
32-35	A_0-A_3	I/O address bus
36	$\overline{EOP}$	I/O end of process
37-40	A_4-A_7	Output address bus

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Pin Functions

D_0-D_7 (I/O Data Bus)

During an I/O read, the CPU enables these lines as outputs, allowing it to read an address register, a word count register, or the status or temporary register. During an I/O write, these lines are enabled as inputs, allowing the CPU to program the μPD8237A control registers. During DMA cycles, the eight MSBs of the address are output to the data bus to be strobed to an external latch via ADDSTB.

A_4-A_7 (Output Address Bus)

These lines, active only during DMA service, are outputs that provide the four MSBs of the address.

A_0-A_3 (I/O Address Bus)

During DMA active states, these lines are outputs that provide the 4 LSBs of the output address bus. During DMA idle states, these lines are inputs, allowing the CPU to load or examine control registers.

DRQ_0-DRQ_3 (DMA Request Input)

These are asynchronous channel request inputs used by peripherals to request DMA service. In a fixed priority scheme, DRQ_3 has the lowest. The polarity of these lines is programmable; however, reset initializes them to active high.

HLDA (Hold Acknowledge)

Indicates that the CPU has relinquished control of the system buses.

HRQ (Hold Request)

Requests control of the system bus. The μPD8237A issues this signal in response to software requests or DRQ inputs from peripherals.

$DACK_0$-$DACK_3$ (DMA Acknowledge Output)

These lines indicate an active channel. They are sometimes used to select a peripheral. Only one DACK may be active at any time. All DACK lines are inactive unless DMA has control of the bus. The polarity of these lines is programmable; however, reset initializes them to active low.

$\overline{EOP}$ (End of Process)

$\overline{EOP}$ signals that DMA service has been completed. When the word count of a channel becomes zero, the μPD8237A pulses $\overline{EOP}$ low to notify the peripheral that DMA service is complete. The peripheral may pull $\overline{EOP}$ low to prematurely end DMA service. Internal or external receipt of $\overline{EOP}$ causes the currently active channel to end service, set its TC bit in the status register, and reset its request bit. If the channel is programmed for autoinitialization, the current registers are updated from the base registers. Otherwise, the channel's mask bit is set and the contents of the register are unaltered.

$\overline{EOP}$ is output when TC for channel 1 occurs during memory-to-memory transfers. $\overline{EOP}$ applies to the channel with an active DACK. When $DACK_0$-$DACK_3$ are inactive, external $\overline{EOP}$s are ignored.

Use of an external pull-up resistor of 3.3 kΩ or 4.7 kΩ is recommended. This pin ($\overline{EOP}$) cannot sink the current passed by a 1 kΩ or 4.7 kΩ pull-up.

RESET

Clears the command, status, request, and temporary registers, the first/last flip flop, and sets the mask register. The μPD8237A is in idle state after a reset.

$\overline{CS}$ (Chip Select)

The CPU uses $\overline{CS}$ to select the μPD8237A as an I/O device during an I/O read or write by the CPU. This provides CPU communication on the data bus. $\overline{CS}$ may be held low during multiple transfers to or from the μPD8237A as long as $\overline{I/OR}$ or $\overline{I/OW}$ is toggled following each transfer.

READY

This signal can extend memory read and write pulses for slow memories or I/O peripherals.

CLK (Clock)

Controls internal operations and data transfer rate.

AEN (Address Enable)

This signal allows the external latch to output the upper address byte by disabling the system bus during DMA cycles. Use HLDA and AEN to deselect I/O peripherals that may be erroneously accessed during DMA transfers. The μPD8237A deselects itself during DMA transfers.

ADDSTB (Address Strobe)

This signal strobes the upper address byte form D_0-D_7 into an external latch.

$\overline{\text{MEMR}}$ (Memory Read)

This signal accesses data from a specified memory location during memory-to-peripheral or memory-to-memory transfers.

$\overline{\text{MEMW}}$ (Memory Write)

This signal writes data to a specified memory location during peripheral-to-memory or memory-to memory transfers.

$\overline{\text{I/OR}}$ (I/O Read)

In the idle state, this signal is an input control line used by the CPU to read control registers. In the active state, the μPD8237A uses $\overline{\text{I/OR}}$ as an output control signal to access data from a peripheral during a DMA write.

$\overline{\text{I/OW}}$ (I/O Write)

In the idle state, the CPU uses $\overline{\text{I/OW}}$, as an input control signal to load information to the μPD8237A. In the active state, the μPD8237A uses $\overline{\text{I/OW}}$ as an output control signal to load data to a peripheral during a DMA read.

The rising edge of $\overline{\text{WR}}$ must follow each data byte transfer in order for the CPU to write to the μPD8237A. Holding $\overline{\text{I/OW}}$ low while toggling $\overline{\text{CS}}$ does not produce the same effect.

Pin 5

Pin 5 is always tied high.

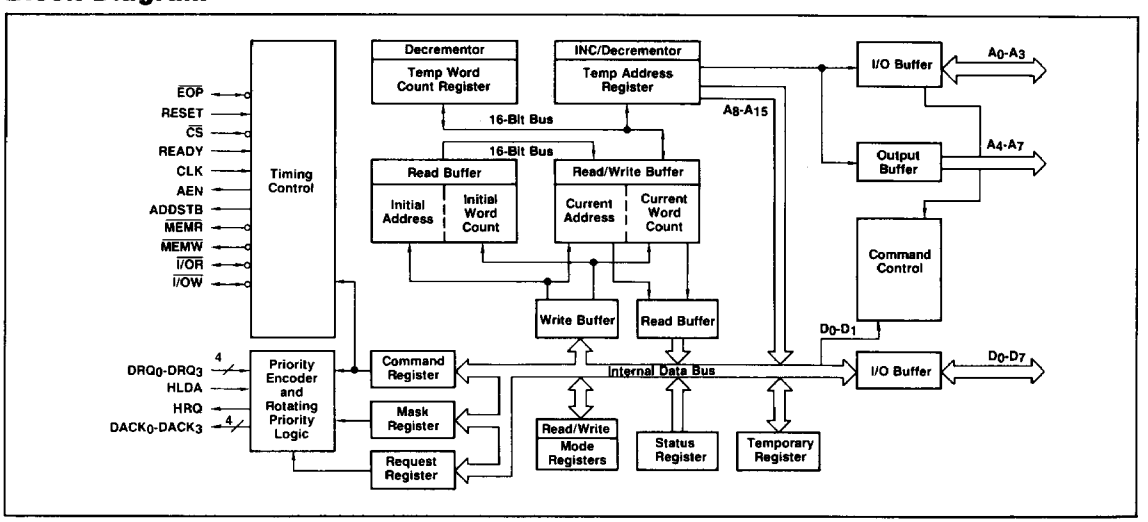
V_{CC}

Power supply.

GND

Ground.

Block Diagram



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Functional Description

The μPD8237A has three basic control logic blocks, as shown in the block diagram. The command control block decodes commands issued by the CPU to the μPD8237A before DMA requests are serviced. It also decodes the mode control word of each channel. The timing control block generates the external control signals and the internal timing. The priority encoder block settles priority contentions among channels simultaneously requesting service.

DMA Operation

The μPD8237A operates in two states: idle and active. Each of these is made up of several smaller states equal to one clock cycle. The inactive state, S1, is entered when there are no pending DMA requests. The controller is inactive in S1, but the CPU may program it. S0 is the initial state for DMA service; the μPD8237A requests a hold, but the CPU has not acknowledged. Transfers may begin upon acknowledgement from the CPU. The normal working states of DMA service are S1, S2, S3, and S4. If more time is needed for a transfer, a wait state, SW, can be inserted using the READY line.

A memory-to-memory transfer requires read-from-memory and write-to-memory operations. The states S11, S12, S13, and S14 provide the read-from operation. S21, S22, S23, and S24 provide the write-to part of the transfer. The byte is stored in the temporary register between operations.

Idle State

When there are no pending service requests, the μPD8237A is in the idle state; more specifically, in S1, DRQ lines and $\overline{CS}$ are sampled to determine requests for DMA service and CPU attempts to inspect or modify the registers of the μPD8237A, respectively. The CPU can read or write to the registers when $\overline{CS}$ and HLDA are low. A_0-A_3 are used as inputs to the μPD8237A and select the registers affected. The $\overline{I/OR}$ and $\overline{I/OW}$ lines select and time the reads and writes. An internal flip-flop generates an additional address bit which determines the upper or lower byte of the address and word count registers. This flip-flop can be reset by master clear, reset, or a software command.

When $\overline{CS}$ and HLDA are low (program phase), the μPD8237A can execute special software commands. When $\overline{CS}$ and $\overline{I/OW}$ are active, the commands are decoded as addresses and do not use the data bus.

Active State

When a channel requests service while the μPD8237A is in idle state, the μPD8237A outputs an HRQ to the CPU and enters the active state. DMA service takes place in the active state, in one of the four modes described below.

DRQ is held active only until the corresponding DACK goes active when a single transfer is performed. If DRQ is held active for a longer period, HRQ will become inactive after each transfer, become active again, and a one-byte transfer will be made after each rising edge of HLDA. This assures a full machine cycle between DMA transfers in 8080A/8085A systems. Timing between the μPD8237A and other bus control protocols depends on the CPU being used.

Block Transfer Mode

In this mode, the μPD8237A makes transfers until it encounters a TC or an external $\overline{EOP}$. Hold DRQ active only until DACK goes active. The channel will autoinitialize at the end of the DMA service if it has been programmed to do so.

Demand Transfer Mode

In this mode, the μPD8237A makes transfers until it encounters a TC or an external $\overline{EOP}$, or until DRQ becomes inactive. This allows the device requesting service to stop the transfers by sending DRQ inactive. The device can resume service by making DRQ active. The current address and current word count registers may be examined during the time between services when the CPU is allowed to operate. Autoinitialization can occur only after a TC or $\overline{EOP}$ at the end of the DMA service. After an autoinitialization, there must be an active-going DRQ edge to begin new DMA service.

Cascade Mode

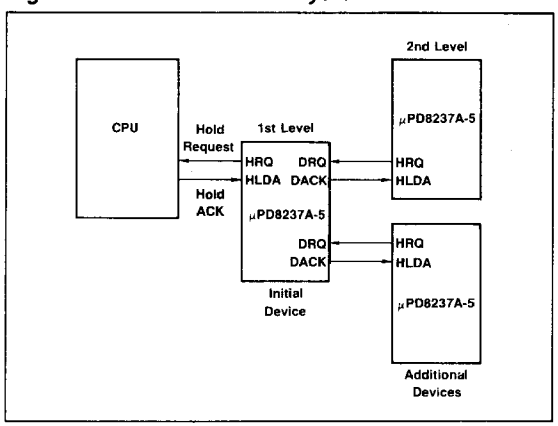
In this mode, you can expand your system by cascading several μPD8237As together. Connect the HLDA and HRQ signals from the additional μPD8237As to the DRQ and DACK signals of a channel of the initial μPD8237A. This scheme allows the additional devices to send the DMA requests through the priority resolution circuitry of the preceding device, preserving the priority chain and forcing the device to wait its turn to acknowledge requests. The cascade channel in the initial device does not output any address or control signals because its only function is that of assigning priorities. The μPD8237A responds to DRQ with DACK, but all outputs except HRQ are disabled.

Figure 1 shows two μPD8237As cascaded into two channels of another one, forming a two-level DMA system. You could add more devices at the second level by using the leftover channels of the first level; likewise, you could add more devices to form a third level by cascading into the channels of the second level.

Transfers

There are three types of transfers that can be performed by the three active transfer modes: read, write, and verify. Read transfers activate $\overline{\text{MEMR}}$ and $\overline{\text{I/OW}}$ to move memory data to an I/O device. Write transfers activate $\overline{\text{I/OR}}$ and $\overline{\text{MEMW}}$ to move data from an I/O device to memory. Verify transfers are not really transfers; the μPD8237A goes through the motions of a transfer but the memory and I/O lines are not active.

Figure 1. Two-Level DMA System



Memory-to-Memory Transfers

Use block transfer mode for memory-to-memory transfers. Mask out channels 0 and 1, and initialize the channel 0 word count to the same value as channel 1. Setting bit C0 of the command register to 1 makes channels 0 and 1 operate as memory-to-memory transfer channels. Channel 0 is the source address, channel 1 is the destination address, and the channel 1 word count is used. Initiate the memory-to-memory transfer by setting a DMA request for channel 0. You can write a single source word to a block of memory when channel 0 is programmed for a fixed source address. The μPD8237A responds to external $\overline{\text{EOP}}$ signals during these transfers, but no DACK outputs are active. The $\overline{\text{EOP}}$ input may be used by data comparators doing block searches to end service when a match is found.

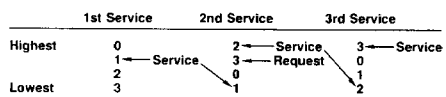
Autoinitialization

A channel may be set for autoinitialize by programming a bit in the mode register. Autoinitialize restores the original values of the current address and current word count registers from the initial address and initial word count registers of that channel. The CPU loads the current and initial registers simultaneously and they are unchanged through DMA service. $\overline{\text{EOP}}$ does not set the mask bit when the channel is in autoinitialize. The channel can repeat its service following autoinitialize without CPU intervention.

Priority Resolution

Two software-selectable priority resolution schemes are available on the μPD8237A: fixed priority and rotating priority. In the fixed priority scheme, priority is assigned by the value of the channel number. Channel 3 is the lowest priority and channel 0 is the highest priority.

In the rotating priority scheme, the channel that was just serviced assumes the lowest priority and the other channels move up accordingly. This guarantees that a device requesting service can be adcknowledged after no more than three other devices have been serviced, preventing any channel from monopolizing the system.



The highest priority channel is selected on each active-going HLDA edge. Once service to a channel begins, it cannot be interrupted by a request from a higher priority channel. A higher priority channel gets control only when the lower priority channel releases HRQ. The CPU gets bus control when control passes from channel to channel, ensuring that a rising HLDA edge can be generated to select the new highest priority request.

Transfer Timing

If, you can cut transfer timing, by compressing the transfer time to two clock periods. Since state 3 (S3) extends the access time for the read pulse, you can eliminate S3, making the width of the read pulse equal to the write pulse. A transfer is then made up of S2 to change the address and S4 to perform the read or write. When the address lines A_8-A_{15} need to be updated, S1 states occur.

Generating Addresses

The eight MSBs of the address are multiplexed on the data lines. These bits are output to an external latch during S1, after which they can be placed on the address bus. The falling edge of ADDSTB loads the bits from the data lines to the latch. AEN places the bits on the address bus. The eight LSBs of the address are directly output on lines A_0-A_7 to the address bus.

Sequential addresses are generated during block and demand transfer mode operations because they include several transfers. Often, data in the external address latch does not change; it changes only when a carry or borrow from A_7 to A_8 occurs in the sequence of addresses. S1 states are executed only when A_8-A_{15} need to be updated. In the course of lengthy transfers, S1 states may be executed only once every 256 transfers.

Registers

Table 1 summarizes the registers of the μPD8237A.

Table 1. Register Summary

Register	No.	Bits
Current address registers	4	16
Current word count registers	4	16
Initial address registers	4	16
Initial word count registers	4	16
Command register	1	8
Mode registers	4	6
Request register	1	4
Mask register	1	4
Status register	1	8
Temporary register	1	8
Temporary address register	1	16
Temporary word count register	1	16

Current Address Register. There is a current address register for each channel. This register holds the address used for DMA transfers; the address is incremented or decremented after each transfer and the intermediate values are stored here during the transfer. The CPU writes or reads this register in 8-bit bytes. An autoinitialize restores this register to its initial value.

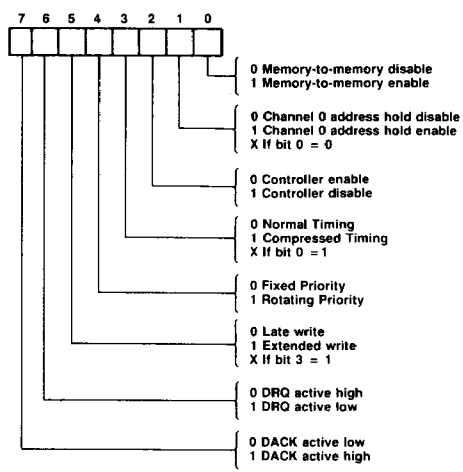
Current Word Count Register. There is a current word count register for each channel. Program this register with the value of the number of words to be transferred, minus one. The word count is decremented after each transfer and intermediate values are stored in this register during the transfer. A TC is generated when the word count is zero. The CPU writes or reads this register in 8-bit bytes during program phase. An autoinitialize restores this register to its initial value. After an internally generated $\overline{EOP}$, the contents of this register with be FFFFH.

Initial Address and Initial Word Count Registers. There is an initial register and an initial word count register for each channel. The initial values of the associated current registers are stored in these registers. The values in these registers are used to restore the current registers at autoinitialize. During DMA programming, the CPU writes the initial registers and the corresponding current registers at the same time, in 8-bit bytes. Intermediate values in the current registers are overwritten if you write to the initial registers while the current registers contain intermediate values. The CPU cannot read the initial registers.

Table 2. Word Count and Address Register Command Codes

Channel	Operation	Signals							Internal Flip-Flop	D_0-D_7
		$\overline{CS}$	$\overline{I/OR}$	$\overline{I/OW}$	A_3	A_2	A_1	A_0		
0	Initial & current address write	0	1	0	0	0	0	0	0	A_0-A_7
		0	1	0	0	0	0	0	1	A_8-A_{15}
	Current address read	0	0	1	0	0	0	0	0	A_0-A_7
		0	0	1	0	0	0	0	1	A_8-A_{15}
	Initial & current word count write	0	1	0	0	0	0	1	0	W_0-W_7
		0	1	0	0	0	0	1	1	W_8-W_{15}
	Current word count read	0	0	1	0	0	0	1	0	W_0-W_7
		0	0	1	0	0	0	1	1	W_8-W_{15}
1	Initial & current address write	0	1	0	0	0	1	0	0	A_0-A_7
		0	1	0	0	0	1	0	1	A_8-A_{15}
	Current address read	0	0	1	0	0	1	0	0	A_0-A_7
		0	0	1	0	0	1	0	1	A_8-A_{15}
	Initial & current word count write	0	1	0	0	0	1	1	0	W_0-W_7
		0	1	0	0	0	1	1	1	W_8-W_{15}
	Current word count read	0	0	1	0	0	1	1	0	W_0-W_7
		0	0	1	0	0	1	1	1	W_8-W_{15}
2	Initial & current address write	0	1	0	0	1	0	0	0	A_0-A_7
		0	1	0	0	1	0	0	1	A_8-A_{15}
	Current address read	0	0	1	0	1	0	0	0	A_0-A_7
		0	0	1	0	1	0	0	1	A_8-A_{15}
	Initial & current word count write	0	1	0	0	1	0	1	0	W_0-W_7
		0	1	0	0	1	0	1	1	W_8-W_{15}
	Current word count read	0	0	1	0	1	0	1	0	W_0-W_7
		0	0	1	0	1	0	1	1	W_8-W_{15}
3	Initial & current address write	0	1	0	0	1	1	0	0	A_0-A_7
		0	1	0	0	1	1	0	1	A_8-A_{15}
	Current address read	0	0	1	0	1	1	0	0	A_0-A_7
		0	0	1	0	1	1	0	1	A_8-A_{15}
	Initial & current word count write	0	1	0	0	1	1	1	0	W_0-W_7
		0	1	0	0	1	1	1	1	W_8-W_{15}
	Current word count read	0	0	1	0	1	1	1	0	W_0-W_7
		0	0	1	0	1	1	1	1	W_0-W_{15}

Command Register. The CPU programs this register during program phase. The register can be cleared with reset.



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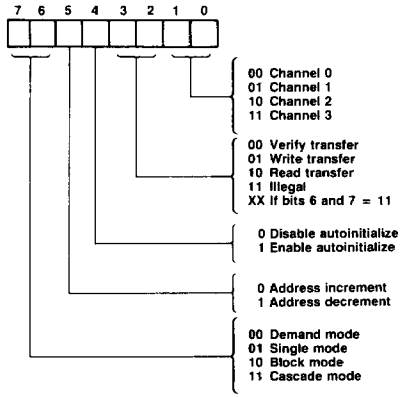
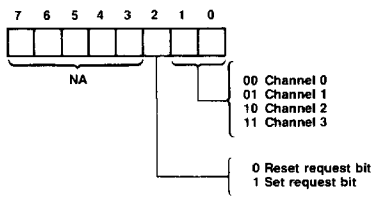
Mode Register. There is a mode register associated with each channel. When the CPU writes to this register during the program phase, bits 0 and 1 determine on which channel mode register the operation is performed.

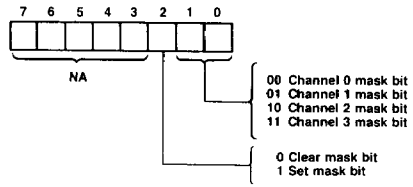


Request Register. This register allows the μPD8237A to respond to DMA requests from software as well as hardware. There is a bit pattern for each channel in the request register. These bits can be prioritized by the priority resolving circuitry and are not maskable. Each bit is set or reset under software control or cleared when TC or an external $\overline{EOP}$ is generated. A reset clears the entire register. The correct data word is loaded by software to set or reset a bit.

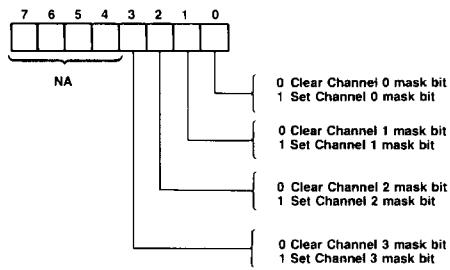
Software requests receive service only when the channel is in block mode. The software request for channel 0 should be set at the beginning of a memory-to-memory transfer.



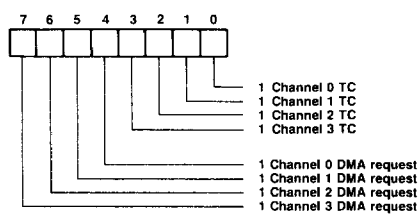
Mask Register. There is a mask bit for each channel which can disable an incoming DRQ. If the channel is not set for autoinitialize, each mask bit is set when its channel produces an $\overline{EOP}$. Each bit can be set or cleared under software control. Reset clears the register. This disallows DMA requests until they are permitted by a clear mask register instruction.



You may also write all four bits of the mask register with a single command.



Status Register. The status register indicates which channels have made DMA requests and which channels have reached TC. Each time a channel reaches TC, including after autoinitialization, bits 0-3 are set. Status read and reset clear these bits. Bits 4-7 are set when a channel is requesting service. The CPU can read the status register.



Temporary Register. The temporary register holds data during memory-to-memory transfers. The CPU can read the last word moved when the transfer is complete. This register always contains the last byte transferred in a memory-to-memory transfer unless cleared by a reset.

Software Commands

There are two software commands that can be executed in the program phase. These commands are independent of data on the data bus.

Clear First/Last Flip-Flop. You may issue this command before reading or writing any word count or address information. It allows the CPU to access registers, addressing upper and lower bytes correctly by initializing the flip-flop to an identifiable state.

Master Clear. This command produces the same effect as reset. It clears the command, status, request, temporary, and internal first/last flip-flop registers, sets the mask register, and causes the μPD8237A to enter idle state.

Table 3 illustrates address codes for the software commands.

Table 3. Software Command Codes

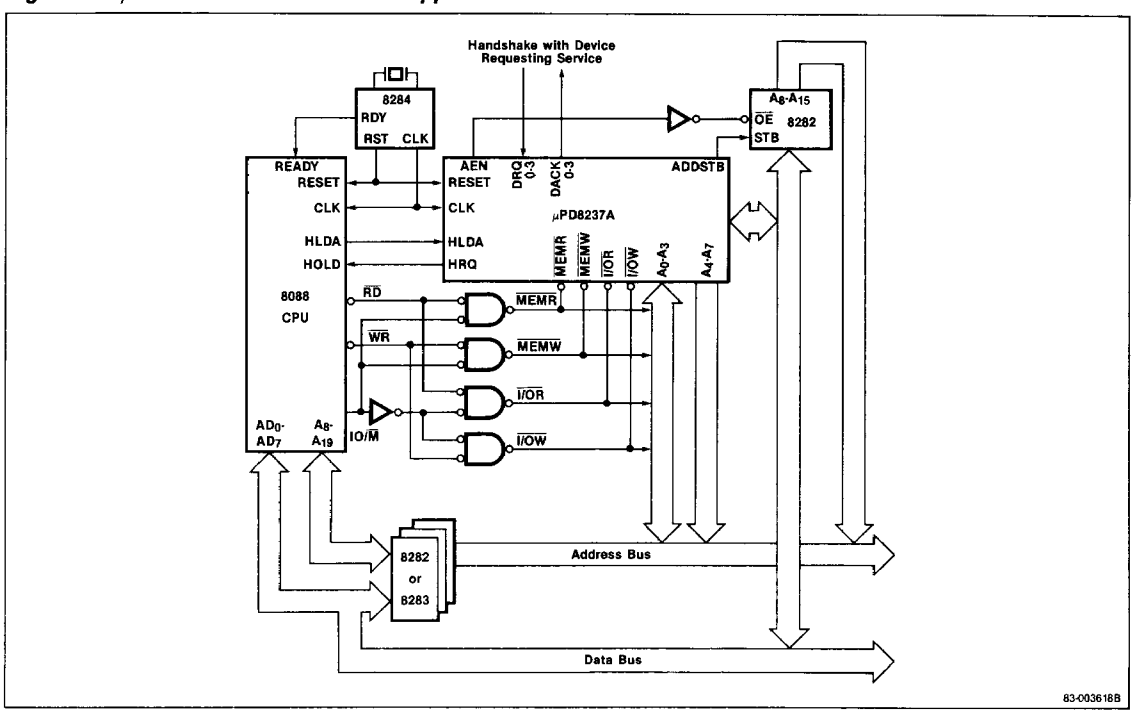
A_3	A_2	A_1	A_0	$\overline{I/OR}$	$\overline{I/OW}$	(1) Operation
1	0	0	0	0	1	Read status register
1	0	0	0	1	0	Write to command register
1	0	0	1	1	0	Write to request register
1	0	1	0	1	0	Write a mask register bit
1	0	1	1	1	0	Write to mode register
1	1	0	0	1	0	Clear byte pointer flip-flop
1	1	0	1	0	1	Read temporary register
1	1	0	1	1	0	Master clear
1	1	1	1	1	0	Write all mask register bits
1	1	1	0	0	1	Clear Mask register

Note:
(1) All other bit combinations are illegal.

Application Example

Figure 2 shows an application using the μPD8237A with an 8088. The μPD8237A sends a hold request to the CPU whenever there is a valid DMA request from a peripheral device. The μPD8237A takes control of the address, data, and control buses when the CPU

Figure 2. μPD8237A DMA Controller Application with 8088 CPU



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replies with an HLDA signal. The address for the first transfer appears in two bytes: the eight LSBs are output on A_0-A_7 and the eight MSBs are output on the data bus pins. The contents of the data bus pins are latched to the 8282 to make up the 16 bits of the address bus. Once the address is latched, the data bus transfers data to or from a memory location or I/O device, using the control bus signals generated by the μPD8237A.

AC Characteristics Supplementary Information

All AC timing measurement points are 2.0 V for high and 0.8 V for low, for both inputs and outputs. The loading on the outputs is one TTL gate plus 100 pF of capacitance for the data bus pins, and one TTL gate plus 50 pF for all other outputs.

Recovery time between successive read and write inputs must be at least 400 ns. I/O or memory write pulse widths will be T_{CY}-100 ns for normal DMA transfers and 2 T_{CY}-100 ns for extended cycles. I/O or memory reads will be 2 T_{CY}-50 ns for normal reads and T_{CY}-50 ns for compressed cycles. T_{DQ1} and T_{DQ2} are measured on two different levels: T_{DQ1} at 2.0 V, T_{DQ2} at 3.3 V with a 3.3 kΩ pull-up resistor. DREQ and DACK are both active high and low. DREQ must be held in the active state (user defined) until DACK is returned from the μPD8237A. The AC waveforms assume these are programmed to the active high state.

Absolute Maximum Ratings

T_A = 25°C

Ambient temperature under bias, T_{OPT}	0°C to +70°C
Storage temperature, T_{STG}	−65°C to +150°C
Voltage on any pin with respect to Ground, V_{CC}	−0.5V to +7V
Power dissipation, P_D	1.5 W

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = 25°C

Parameter	Symbol	Limits Min	Typ(1)	Max	Unit	Test Conditions
Output capacitance	C_O		4	8	pF	fc = 1.0 MHz, Inputs = 0 V
Input capacitance	C_I		8	15	pF	
I/O capacitance	C_{IO}		10	18	pF	

Note:
(1) Typical values measured at T_A = 25°C, nominal processing parameters, and nominal V_{CC}.

DC Characteristics

T_A = 0°C to +70°C; V_{CC} = +5 V ± 5%

Parameter	Symbol	Limits Min	Typ(1)	Max	Unit	Test Conditions
Output high voltage	V_{OH}	2.4			V	I_{OH} = −200 μA
		3.3			V	I_{OH} = −100 μA (HRQ only)
Output low voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA (Data bus)
						I_{OL} = 3.2 mA (Other outputs)
Input high voltage	V_{IH}	2.0		V_{CC} +0.5	V	
Input low voltage	V_{IL}	−0.5		0.8	V	
Input load current	I_{LI}			±10	μA	0V ≤ V_{IN} ≤ V_{CC}
Output leakage current	I_{LO}			±10	μA	0.45 ≤ V_{OUT} ≤ V_{CC}
V_{CC} supply current	I_{CC}		65	130	mA	T_A = +25°C
			75	150	mA	T_A = 0°C

Note:
(1) Typical values measured at T_A = 25°C, nominal processing parameters, and nominal V_{CC}.

AC Characteristics

DMA (Master) Mode

T_A = 0°C to +70°C; V_{CC} = 5V ± 5%; V_{SS} = 0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit
AEN high from CLK low (S1) delay time	t_{AEL}			200	ns
AEN low from CLK high (S1) delay time	t_{AET}			130	ns
ADR active to float delay from CLK high	t_{AFAB}			90	ns
$\overline{READ}$ or $\overline{WRITE}$ float from CLK high	t_{AFC}			120	ns
DB active to float delay from CLK high	t_{AFDB}			170	ns
ADR from $\overline{READ}$ high hold time	t_{AHR}	$t_{CY}-100$			ns
DB from ADDSTB low hold time	t_{AHS}	30			ns
ADR from $\overline{WRITE}$ high hold time	t_{AHW}	$t_{CY}-50$			ns
DACK valid from CLK low delay time	t_{AK}			170	ns
$\overline{EOP}$ high from CLK high delay time	t_{AK}			170	ns
$\overline{EOP}$ low to CLK high delay time	t_{AK}			100	ns
ADR stable from CLK high	t_{ASM}			170	ns
Data bus to ADDSTB low setup time	t_{ASS}	100			ns
Clock high time (transitions ≤ 10 ns)	t_{CH}	80			ns
Clock low time (transitions ≤ 10 ns)	t_{CL}	68			ns
CLK cycle time	t_{CY}	200			ns
CLK high to $\overline{READ}$ or $\overline{WRITE}$ low delay(1)	t_{DCL}			190	ns
$\overline{READ}$ high from CLK high (S-4) delay time(1)	t_{DCTR}			190	ns
$\overline{WRITE}$ high from CLK high (S-4) delay time(1)	t_{DCTW}			130	ns
HRQ valid from CLK high delay time(2)	t_{DQ1} t_{DQ2}			120 120	ns ns
$\overline{EOP}$ low from CLK low setup time	t_{EPS}	40			
$\overline{EOP}$ pulse width	t_{EPW}	220			ns
ADR float to active delay from CLK high	t_{FAAB}			170	ns
$\overline{READ}$ or $\overline{WRITE}$ active from CLK high	t_{FAC}			150	ns
Data bus float to active delay from CLK high	t_{FADB}			200	ns
HLDA valid to CLK high setup time	t_{HS}	75			ns
Input data from $\overline{MEMR}$ high hold time	t_{IDH}	0			ns
Input data to $\overline{MEMR}$ high setup time	t_{IDS}	170			ns
Output data from $\overline{MEMW}$ high hold time	t_{ODH}	10			ns
Output data valid to $\overline{MEMW}$ high	t_{ODV}	125			ns
DRQ to CLK low (S1, S4) setup time	t_{QS}	0			ns
CLK to READY low hold time	t_{RH}	20			ns
READY to CLK low setup time	t_{RS}	60			ns
ADDSTB high from CLK high delay time	t_{STL}			130	ns
ADDSTB low from CLK high delay time	t_{STT}			90	ns

Note:

(1) Net $\overline{I/OW}$ or $\overline{MEMW}$ pulse width for normal write is $t_{CY}-100$ ns and $t_{CY}-100$ ns for extended write. Net $\overline{I/OR}$ or $\overline{MEMR}$ pulse width for normal read to $2t_{CY}-50$ ns and $t_{CY}-50$ ns for compressed read.

(2) T_{DQ1} is measured at 2.0 V. t_{DQ2} is measured at 3.3 V. An external pullup resistor of 3.3Ω connected from HRQ to V_{CC} is assumed for t_{DQ2}.

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AC Characteristics (cont)

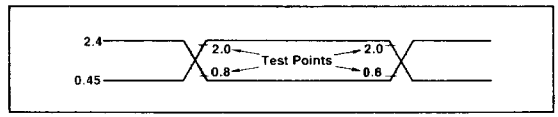
Peripheral Mode

T_A = 0°C to +70°C; V_{CC} = 5 V ± 5%; V_{SS} = 0 V

Parameter	Symbol	Limits			Unit
		Min	Typ	Max	
ADR valid or $\overline{CS}$ low to $\overline{READ}$ low	t_{AR}	50			ns
ADR valid to $\overline{WRITE}$ high setup time	t_{AW}	150			ns
CS low to $\overline{WRITE}$ high setup time	t_{CW}	150			ns
Data valid to $\overline{WRITE}$ high setup time	t_{DW}	150			ns
ADR or CS hold from $\overline{READ}$ high	t_{RA}	0			ns
Data access from $\overline{READ}$ low(1)	t_{RDE}			140	ns
Data bus float delay from $\overline{READ}$ high	t_{RDF}	0		70	ns
Power supply high to RESET low setup time	t_{RSTD}	500			ns
RESET to first I/OR or I/OW	t_{RSTS}	$2t_{CY}$			ns
RESET pulse width	t_{RSTW}	300			ns
$\overline{READ}$ width	t_{RW}	200			ns
ADR from $\overline{WRITE}$ high hold time	t_{WA}	20			ns
CS high from $\overline{WRITE}$ high hold time	t_{WC}	20			ns
Data from $\overline{WRITE}$ high hold time	t_{WD}	30			ns
Write width	t_{WWS}	160			ns

Note:
(1) Data bus output loading is 1 TTL gate plus 100 pF capacitance.

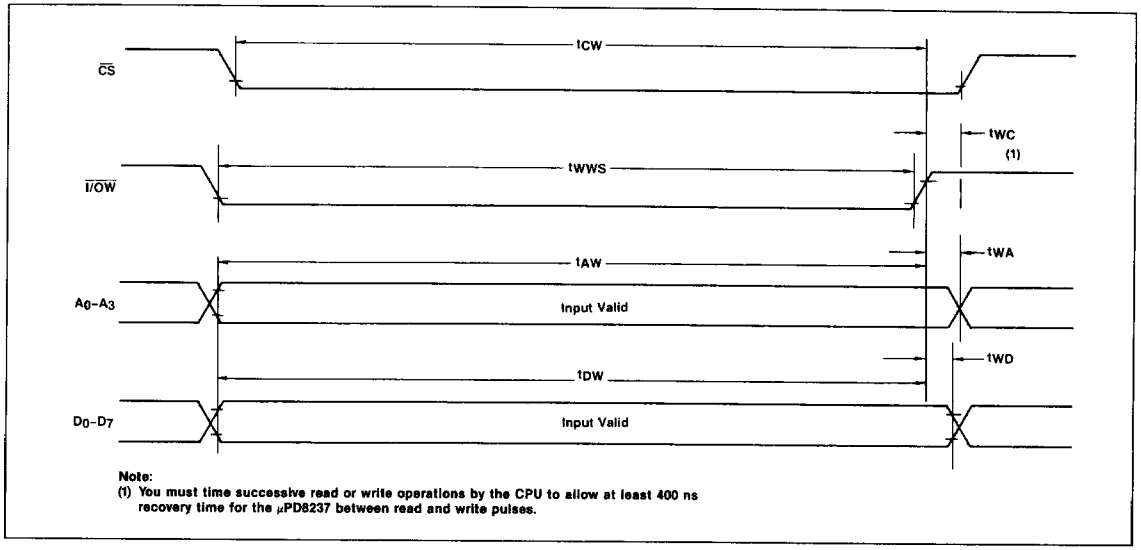
AC Testing Input/Output Waveform



Inputs are driven at 2.4V for logic 1 and 0.45V for logic 0. These timing measurements are made at 2.0V for logic 1 and 0.8V for logic 0. A transition time of 20 ns or less is assumed for input timing parameters. Unless noted, output loading is 1 TTL gate plus 50 pF capacitance.

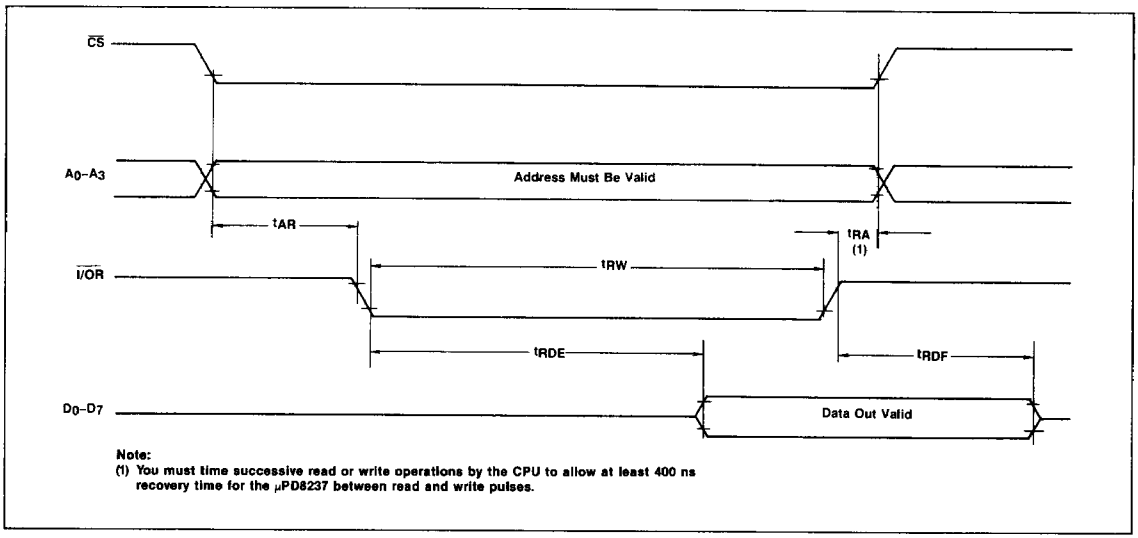
Timing Waveforms

Slave Mode Write



Note:
(1) You must time successive read or write operations by the CPU to allow at least 400 ns recovery time for the μPD8237 between read and write pulses.

Slave Mode Read



Note:
(1) You must time successive read or write operations by the CPU to allow at least 400 ns recovery time for the μPD8237 between read and write pulses.

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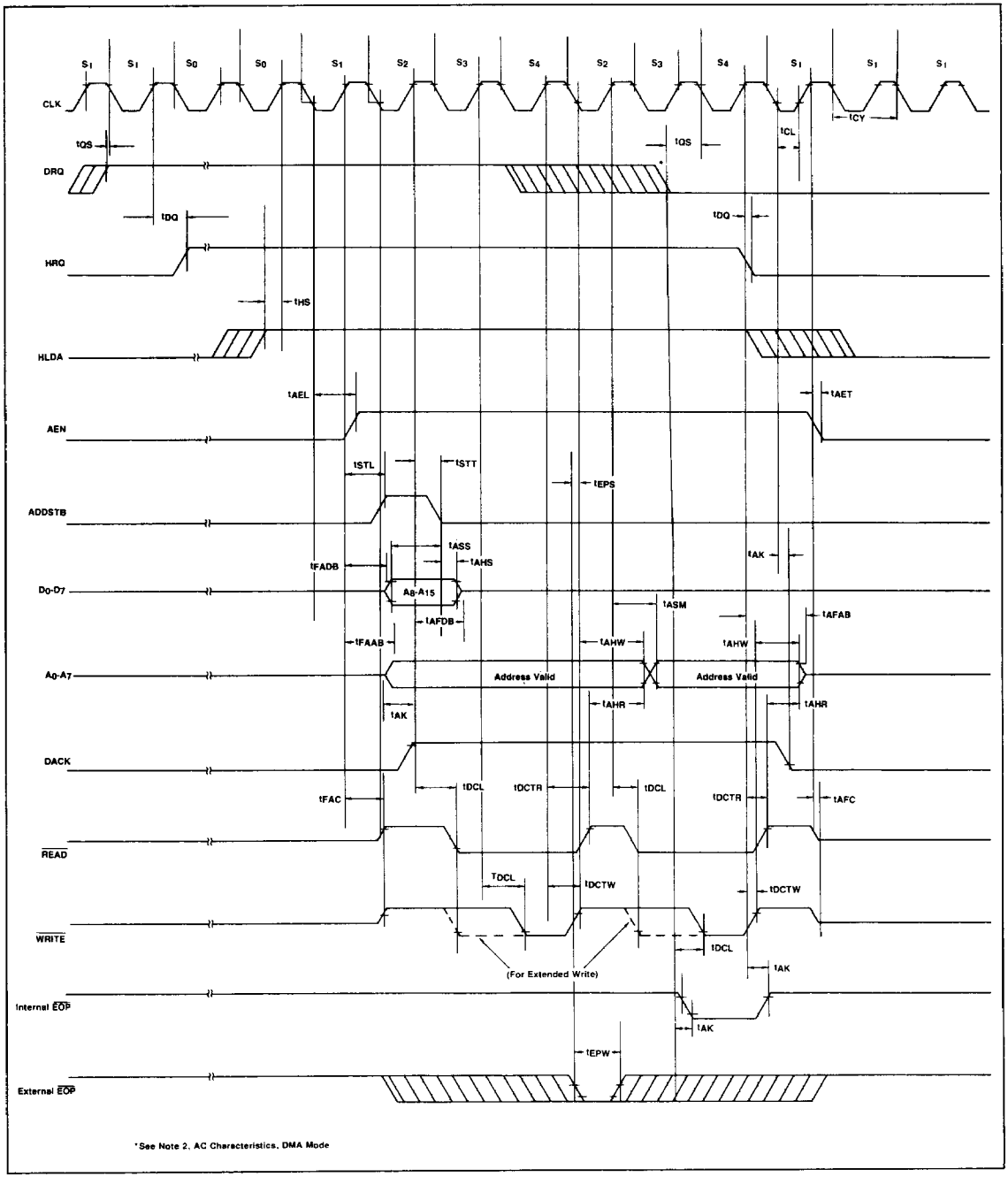
Timing Waveforms (cont)

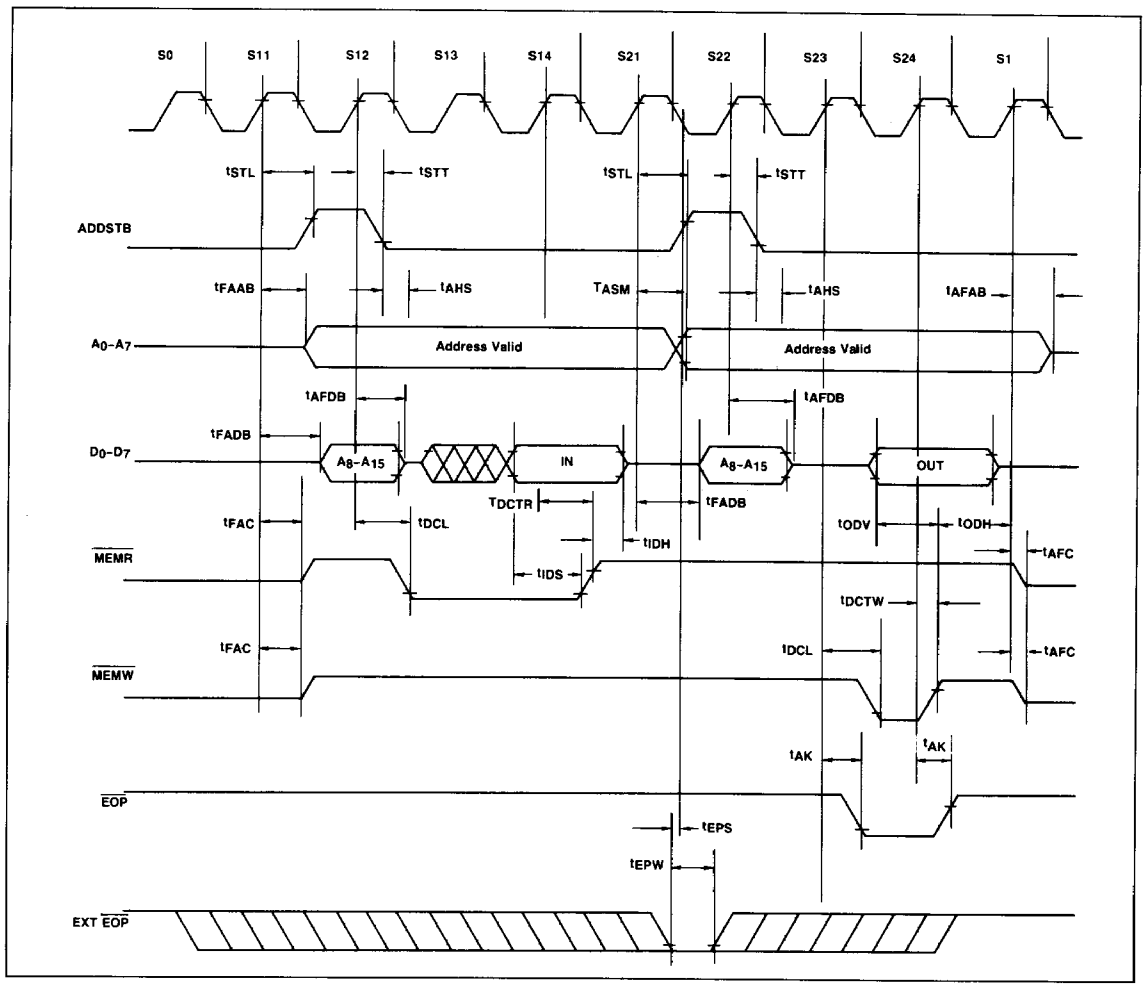
DMA Transfer



*See Note 2, AC Characteristics, DMA Mode

Timing Waveforms (cont)

Memory-to-Memory Transfer



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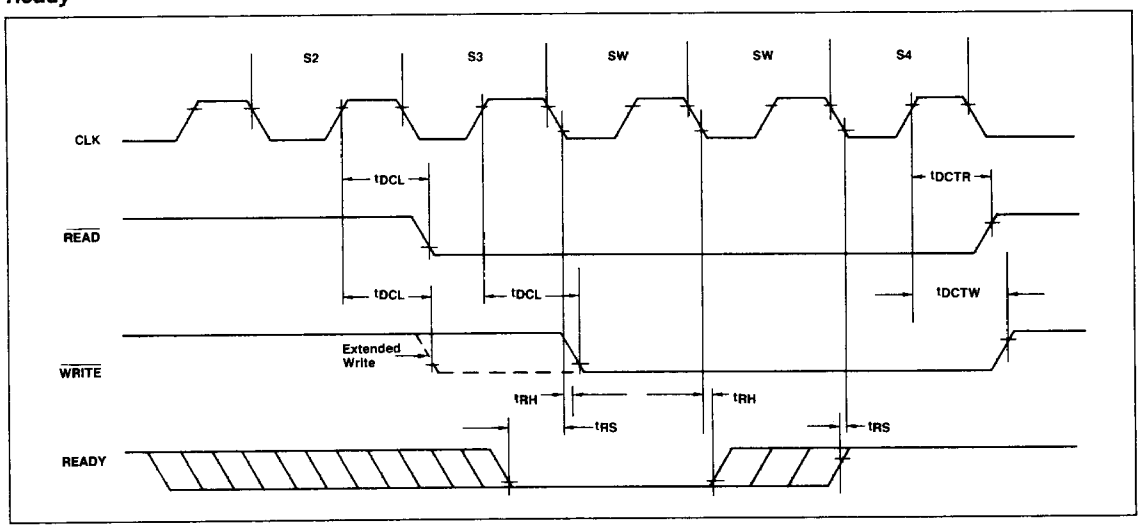
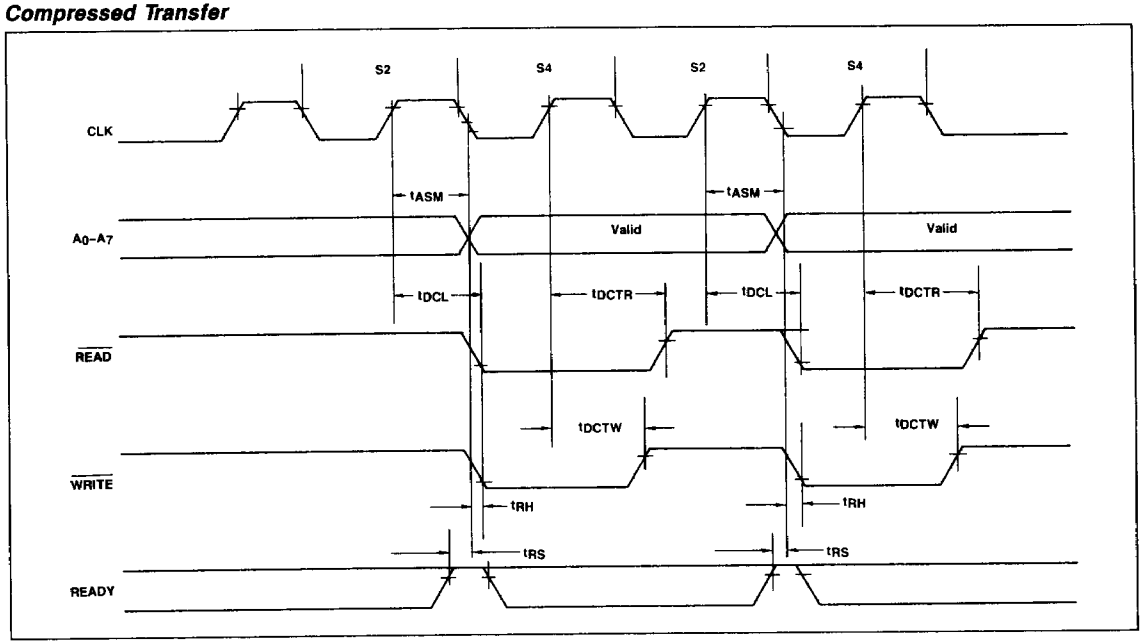
Timing Waveforms (cont)

Ready



Compressed Transfer



Timing Waveforms (cont)

Reset