



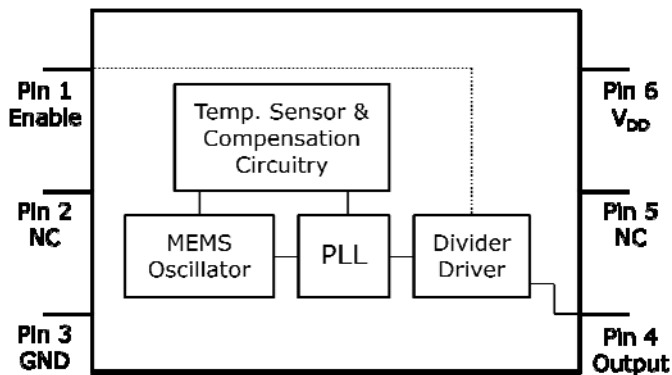
Programmable Low-Jitter Precision CMOS Oscillator

General Description

The DSC8101 & DSC8121 series of high performance field-programmable oscillators utilizes a proven silicon MEMS technology to provide excellent jitter and stability over a wide range of supply voltages and temperatures. Using the TIMEFLASH programmer, the end user can easily program the oscillators' frequency in the field for immediate testing or use in advance prototype development or production.

DSC8101 has a standby feature allowing it to completely power-down when EN pin is pulled low; whereas for DSC8121, only the outputs are disabled when EN is low. Both oscillators are available in industry standard packages, including the small 3.2x2.5 mm², and are "drop-in" replacement for standard 4-pin CMOS quartz oscillators.

Block Diagram



Output Enable Modes

| EN Pin | DSC8101 | DSC8121 |
|--------|---------------|-----------------|
| High | Output Active | Output Active |
| NC | Output Active | Output Active |
| Low | Standby | Output Disabled |

Features

- **Low RMS Phase Jitter: <1 ps (typ)**
- **High Stability: ±10, ±25, ±50 ppm**
- **Wide Temperature Range**
 - Automotive: -55° to 125° C
 - Ext. Industrial: -40° to 105° C
 - Industrial: -40° to 85° C
 - Ext. commercial: -20° to 70° C
- **High Supply Noise Rejection: -50 dBc**
- **Short Lead Time: 2 Weeks**
- **Wide Freq. Range: 10 to 170 MHz**
- **Small Industry Standard Footprints**
 - 3.2x2.5, 5.0x3.2, and 7.0x5.0 mm
- **Excellent Shock & Vibration Immunity**
 - Qualified to MIL-STD-883
- **High Reliability**
 - 20x better MTF than quartz oscillators
- **Low Current Consumption**
- **Supply Range of 2.25 to 3.6 V**
- **Standby & Output Enable Function**
- **Lead Free & RoHS Compliant**

Applications

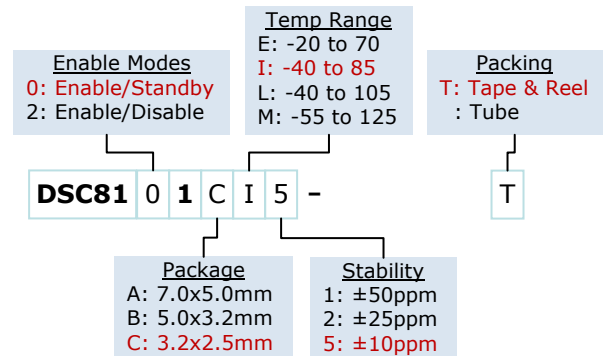
- **Storage Area Networks**
 - SATA, SAS, Fibre Channel
- **Passive Optical Networks**
 - EPON, 10G-EPON, GPON, 10G-PON
- **Ethernet**
 - 1G, 10GBASE-T/KR/LR/SR, and FCoE
- **HD/SD/SDI Video & Surveillance**
- **PCI Express**
- **DisplayPort**

Absolute Maximum Ratings

| Item | Min | Max | Unit | Condition |
|----------------|------|--------------|------|------------|
| Supply Voltage | -0.3 | +4.0 | V | |
| Input Voltage | -0.3 | $V_{DD}+0.3$ | V | |
| Junction Temp | - | +150 | °C | |
| Storage Temp | -55 | +150 | °C | |
| Soldering Temp | - | +260 | °C | 40sec max. |
| ESD | - | | V | |
| HBM | | 4000 | | |
| MM | | 400 | | |
| CDM | | 1500 | | |

Note: 1000+ years of data retention on internal memory

Ordering Code

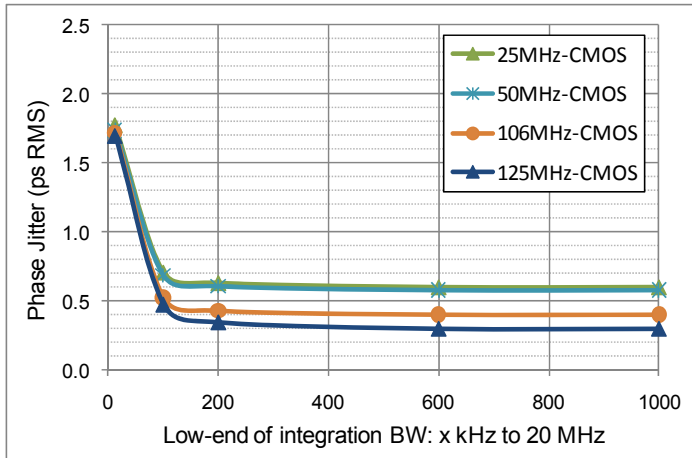


Specifications

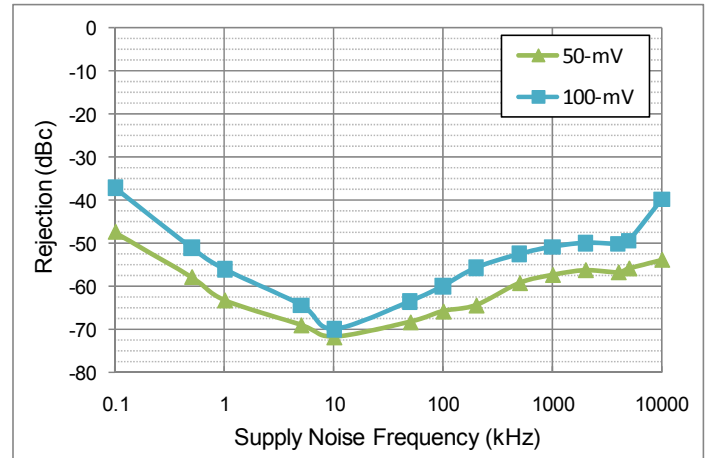
| Parameter | Condition | Min. | Typ. | Max. | Unit |
|--|--|---------------------|--------------------|---------------------|-------------------|
| Supply Voltage ¹ | V_{DD} | 2.25 | | 3.6 | V |
| Supply Current | I_{DD} EN pin low – output is disabled DSC8101 DSC8121 | | 20 | 0.095 22 | mA |
| Frequency Stability Ext Comm. & Ind. only All temp ranges All temp ranges | Δf Includes frequency variations due to initial tolerance, temp. and power supply voltage | | | ±10 ±25 ±50 | ppm |
| Aging | Δf 1 year @25°C | | | ±5 | ppm |
| Startup Time ² | t_{SU} T=25°C | | | 5 | ms |
| Input Logic Levels Input logic high Input logic low | V_{IH} V_{IL} | 0.75x V_{DD} - | | - 0.25x V_{DD} | V |
| Output Disable Time ³ | t_{DA} | | | 5 | ns |
| Output Enable Time | t_{EN} DSC8101 DSC8121 | | | 5 20 | ms ns |
| Enable Pull-Up Resistor ⁴ | Pull-up resistor exist | | 40 | | kΩ |
| CMOS Output | | | | | |
| Supply Current ⁴ | I_{DD} output is enabled $C_L=15pF$, $F_0=125$ MHz | | 31 | 35 | mA |
| Output Logic Levels Output logic high Output logic low | V_{OH} V_{OL} I=±6mA | 0.9x V_{DD} - | | - 0.1x V_{DD} | V |
| Output Transition time ³ Rise Time Fall Time | t_R t_F 20% to 80% $C_L=15pF$ | | 1.1 1.3 | 2 2 | ns |
| Frequency | f_0 All temp range except Auto Auto temp range | 10 | | 170 100 | MHz |
| Output Duty Cycle | SYM | 45 | | 55 | % |
| Period Jitter | J_{PER} Fout=125MHz | | 3 | | ps _{RMS} |
| Integrated Phase Noise | J_{PH} 200kHz to 20MHz @ 125MHz 100kHz to 20MHz @ 125MHz 12kHz to 20MHz @ 125MHz | | 0.3 0.38 1.7 | | ps _{RMS} |

- Pin 6 V_{DD} should be filtered with 0.1uF capacitor.
- t_{SU} is time to 100PPM of output frequency after V_{DD} is applied and outputs are enabled.
- Output Waveform and Test Circuit figures below define the parameters.
- Output is enabled if pad is floated or not connected.

Nominal Performance Parameters (Unless specified otherwise: $T=25^{\circ}C$, $V_{DD}=3.3V$)

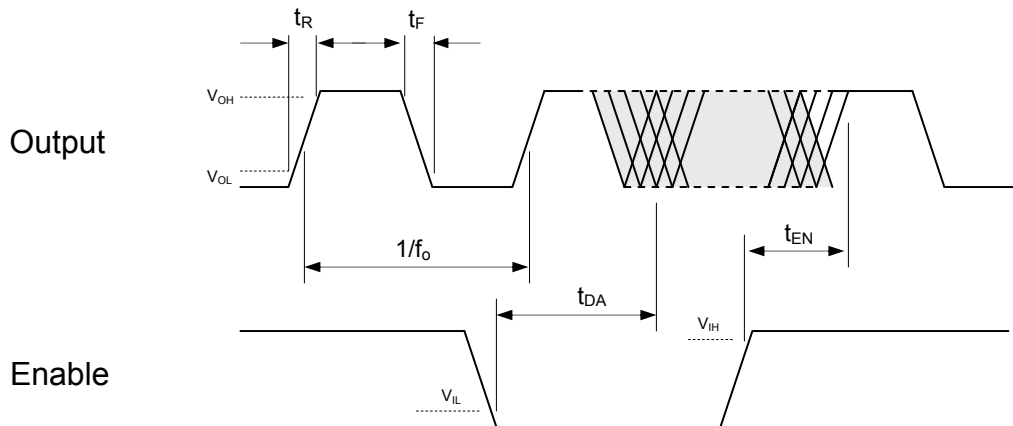


Phase jitter (integrated phase noise)

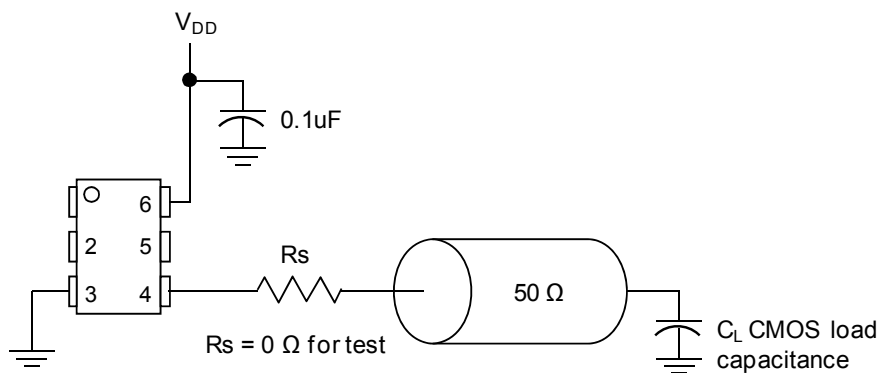


Power supply rejection ratio

Output Waveform

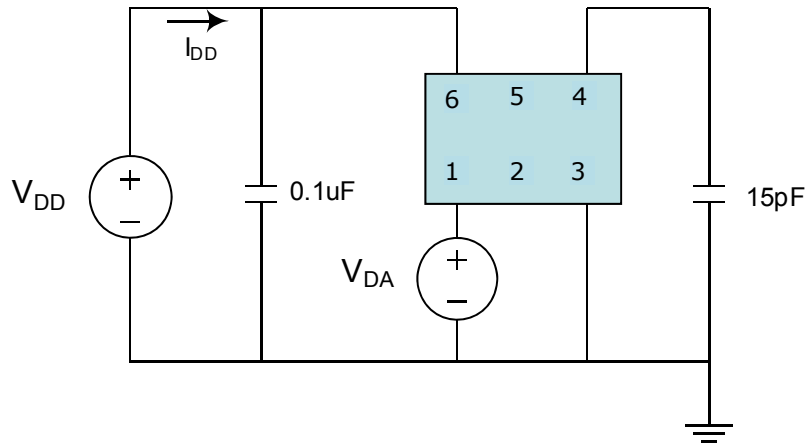


Typical Termination Scheme

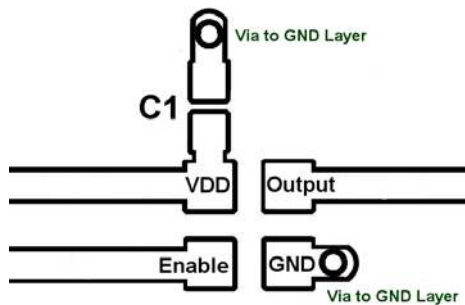


R_s serves to match the trace impedances. Depending on board layout, the value may range from 0 to 30 ohms.

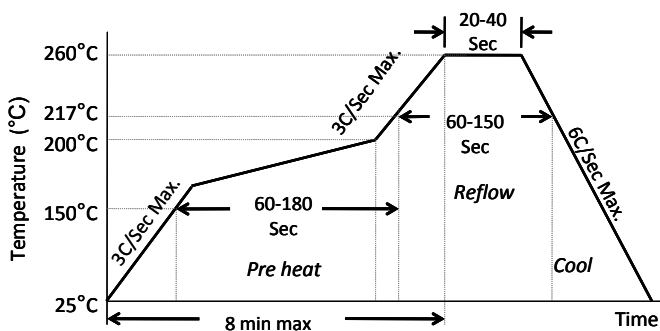
Test Circuit



Board Layout (recommended)



Solder Reflow Profile

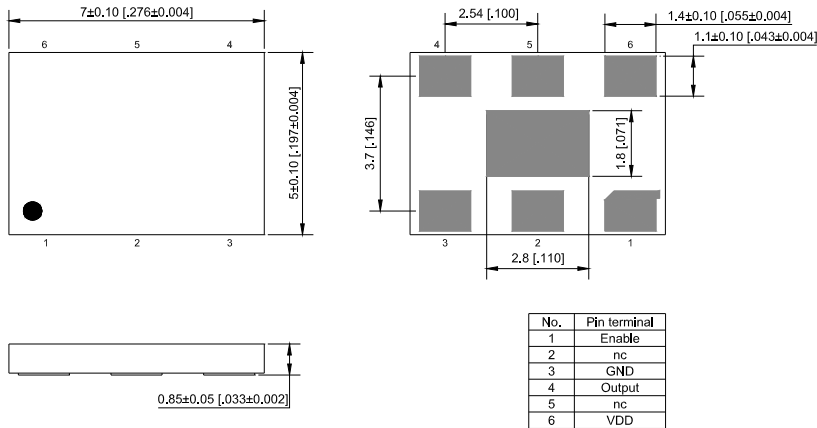


| MSL 1 @ 260°C refer to JSTD-020C | |
|-----------------------------------|--------------|
| Ramp-Up Rate (200°C to Peak Temp) | 3°C/Sec Max. |
| Preheat Time 150°C to 200°C | 60-180 Sec |
| Time maintained above 217°C | 60-150 Sec |
| Peak Temperature | 255-260°C |
| Time within 5°C of actual Peak | 20-40 Sec |
| Ramp-Down Rate | 6°C/Sec Max. |
| Time 25°C to Peak Temperature | 8 min Max. |

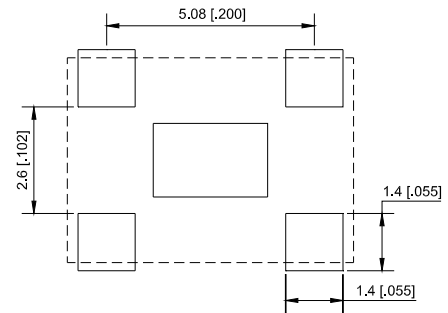
Package Dimensions

7.0 x 5.0 mm Plastic Package

External Dimensions
units: mm[inch]

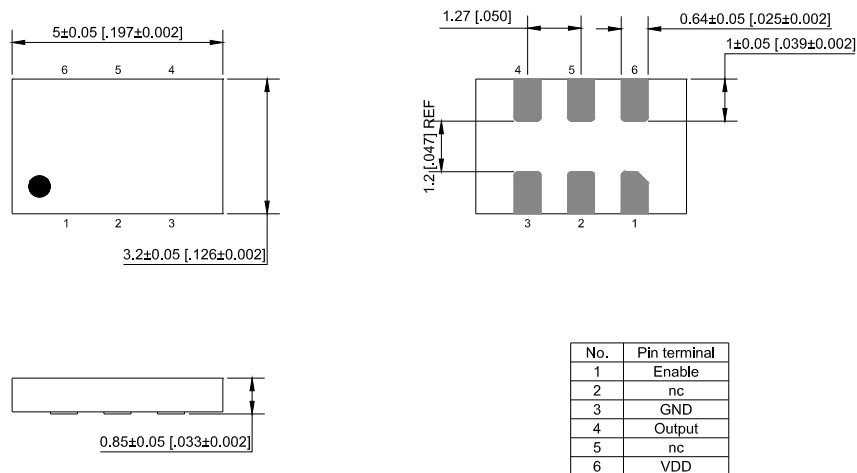


Recommended
Solder Pad Layout
units: mm[inch]

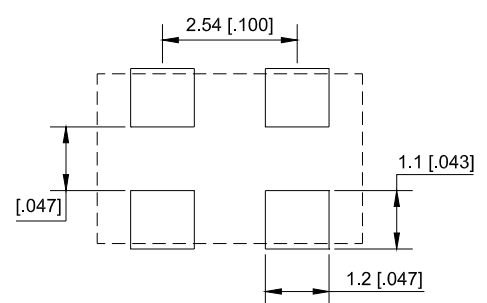


5.0 x 3.2 mm Plastic Package

External Dimensions
units: mm[inch]



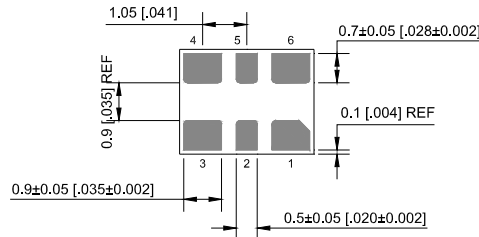
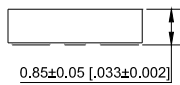
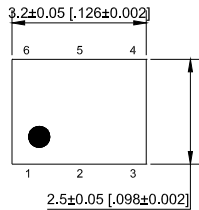
Recommended
Solder Pad Layout
units: mm[inch]



3.2 x 2.5 mm Plastic Package

External Dimensions

units: mm[inch]



| No. | Pin terminal |
|-----|--------------|
| 1 | Enable |
| 2 | nc |
| 3 | GND |
| 4 | Output |
| 5 | nc |
| 6 | VDD |

Recommended Solder Pad Layout

units: mm[inch]

