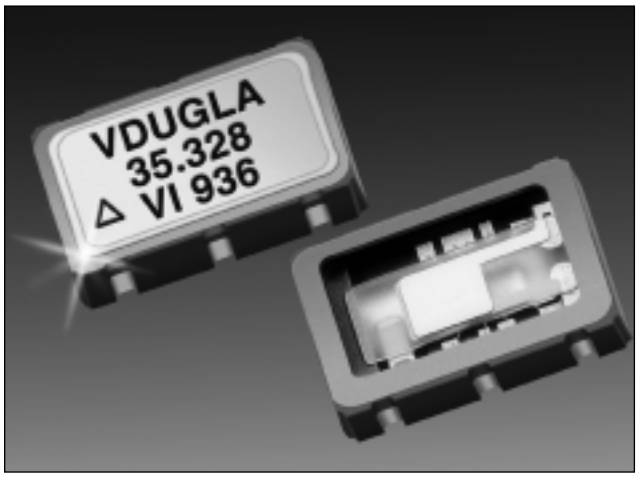
VECTRON INTERNATIONAL
A DOVER TECHNOLOGIES COMPANY

Product Data Sheet

V-Type
Voltage Controlled Crystal Oscillator (VCXO)



Features

- Output Frequencies to 77.760 MHz
- 5.0 or 3.3 volt operation
- Tri-State Output
- Jitter Performance <6 ps rms (freq >12MHz)
- VCXO with SwitchableTTL/CMOS Output
- Robust 6 contact Leadless Ceramic Chip Carrier
- 7.49 x 5.08 x 1.8 mm Surface Mount Device
- Absolute Pull Range Performance to 100 ppm
- Commercial and Industrial Temperature Range
- EIA Compatible Tape and Reel Packaging

Applications

- xDSL Customer Premise Equipment (CPE)
- Cable Modems
- HFC Subscriber Equipmemt
- ATM/SONET/SDH applications

Description

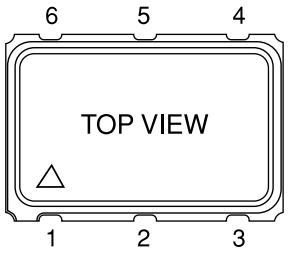
The VI V-Type Voltage Controlled Crystal Oscillator (VCXO) is a quartz-stabilized square-wave generator with selectable TTL or CMOS output. The device is hermetically sealed in a leadless ceramic chip carrier with 6 contact pads.

The V-Type's ultra small footprint and low profile make it ideally suited to applications where space is limited or where backside assembly is required.

Pin Information

Table 1.

Pin #	Symbol	Name/Function
1	Vc	Control Voltage.
2[2]	TTL/CMOS[1]	TTL logic low for CMOS optimized symmetry TTL logic high or no connection for TTL optimized symmetry.
3	GND	Case/circuit ground.
4	Output	Output waveform.
5[2]	Tri-state	TTL logic low diables output. TTL logic high or no connection enables output waveform.
6	V_{DD}	Supply Voltage, 5 V ±10%, or 3.3V ±10%



1. This silicon oscillator is fabricated in CMOS technology and its output waveform will swing between ground and VDD for all but the highest frequency applications. To account for the difference in switching thresholds between TTL logic (1.40 V) and CMOS logic (VDD/2), the TTL/CMOS lead modifies the "on time" of the oscillator for maximum symmetry about the TTL or CMOS logic threshold. TTL logic low provides waveform symmetry for CMOS. TTL logic high or no connection provides waveform symmetry for TTL. At output frequencies less than 12 MHz, this option is not provided as the waveform transition times are small compared to the period. Hence, for f_o <12 MHz this pin should be grounded for electrical isolation.

2. Alternate Pin Configuration for Tri-state Control on Pin 2 and TTL/CMOS on pin 5. Alternate Configuration is indicated by last letter of part code "D" for TriState Pin 2 and TTL/CMOS on pin 5.

Table 2. Performance Specifications

Parameter	Symbol	Min	Max	Unit
Supply Voltage' (5V or 3.3V)	V_{DD}	0.9*V_{DD}	1.1*V_{DD}	V
Supply Current (Frequency Dependent)	I_{DD}	See Figures 7,8		mA
OutputVoltage Levels (V_{DD} = 4.5V): Output Logic High[2] Output Logic Low[2]	 V_{OH} V_{OL}	 0.8*V_{DD} -	 - 0.1*V_{DD}	 V V
Transition Times[2]: Rise Time Fall Time	 t_R t_F		 5 5	 ns ns
Symmetry or Duty Cycle[3]	SYM	See figure 3, 4		%
Nominal Output Frequency (see ordering info)	f_o	1.024	77.760	MHz
Control Voltage (5v), test conditions for APR	V_C	0.5	4.5	V
Control Voltage (3.3v), test conditions for APR	V_C	0.3	3.0	V
Control Voltage	V_C	0	V_{DD}	V
Absolute Pull Range (see ordering info)	APR	±20 to ±100		
Leakage Current of Control Input	I_{VCXO}	-1.0	1.0	uA
Control Voltage Bandwidth (-3 dB,V_C=2.50V)	BW	10	-	kHz

1 A 0.1 uF low frequency tantalum bypass capacitor in parallel with a 0.01 uF high-frequency ceramic capacitor is recommended.

2 Figure 1 defines these parameters. Figure 2 illustrates the equivalent five-gate MTTL load and operating conditions under which these parameters are specified.

3 Symmetry is defined as (ON TIME/PERIOD), with VS = 1.4 V for TTL or VS = 2.5 V for CMOS. per Figure 1.

Table 3: Typical Single-Side Band Phase Noise Data (dBc/Hz)

Offset From Carrier	VCXO Center Frequency						
	6.176MHz	12.288MHz	19.440MHz	32.768MHz	39.3216MHz	44.736MHz	51.840MHz
10 Hz	-80	-70	-70	-68	-63	-63	-63
100 Hz	-109	-100	-100	-98	-93	-93	-93
1 KHz	-134	-129	-129	-125	-122	-122	-122
10 KHz	-147	-145	-145	-147	-144	-144	-144
100 KHz	-152	-152	-152	-152	-151	-151	-151

Electrical Specifications

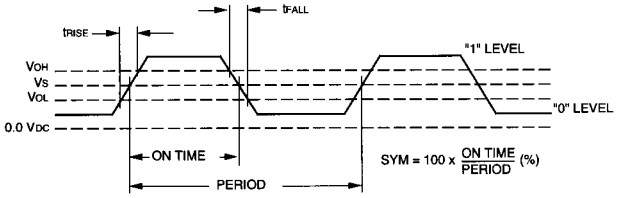
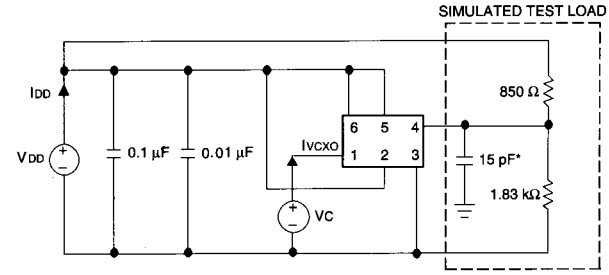


Figure 1. Output Waveform



*Includes probe and test jig capacitance

Figure 2. Output Test Conditions (T_{amb} = 25 ±5°C)

Characteristic Curves

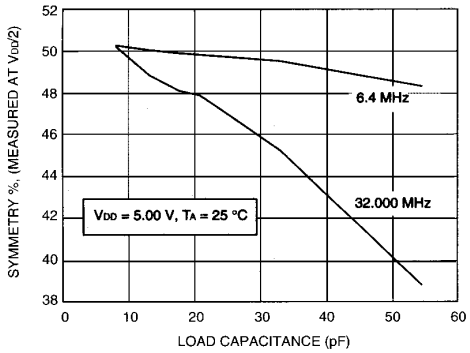


Figure 3. Waveform Symmetry vs. Load Capacitance

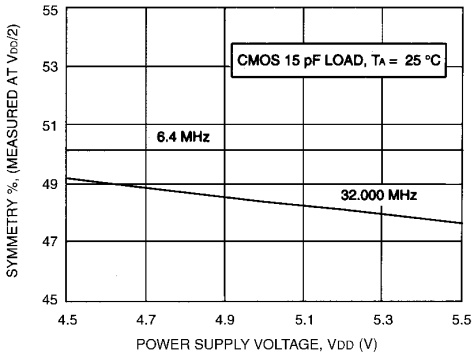


Figure 4. Variation of Duty Cycle with Supply Voltage

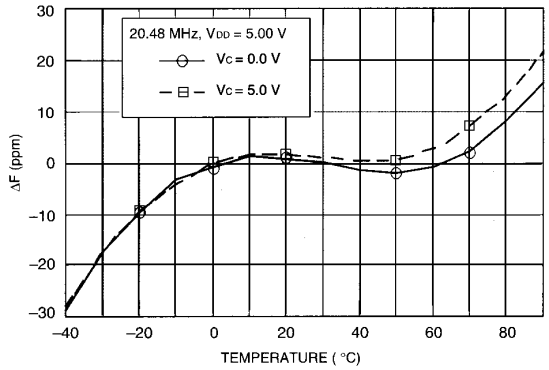


Figure 5. Typical Frequency vs. Temperature

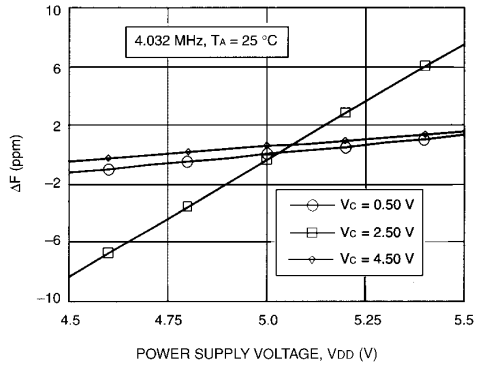


Figure 6. Output Frequency vs. Power Supply Voltage

Characteristic Curves (continued)

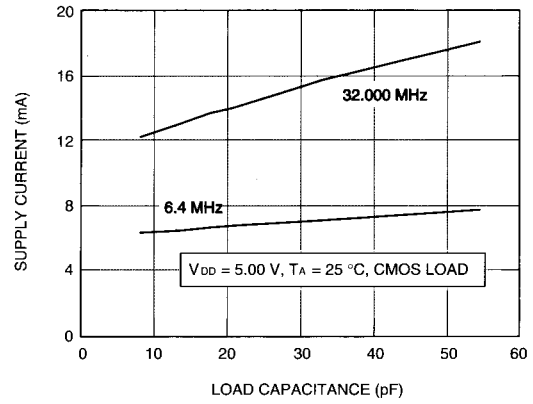


Figure 7. Variation of Supply Current with Capacitive Load

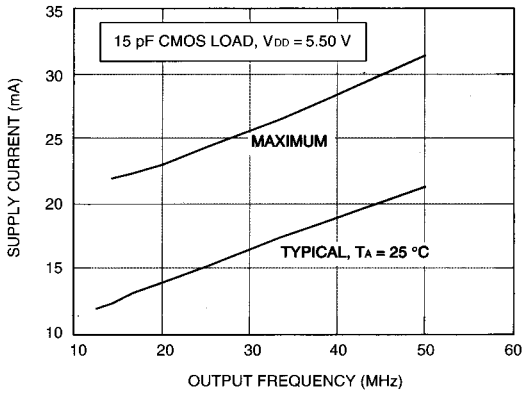


Figure 8. Supply Current vs. Output Frequency

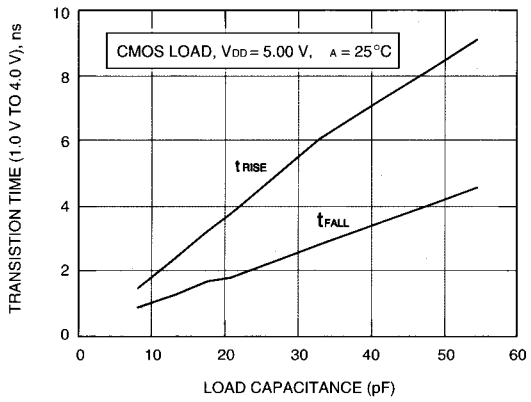


Figure 9. Waveform Transition Times vs. Load Capacitance

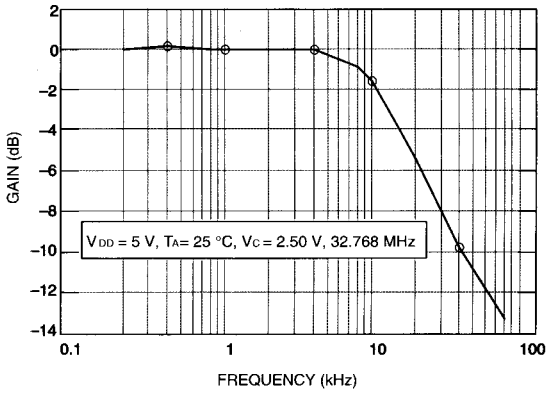


Figure 10. VCXO Input Frequency Response

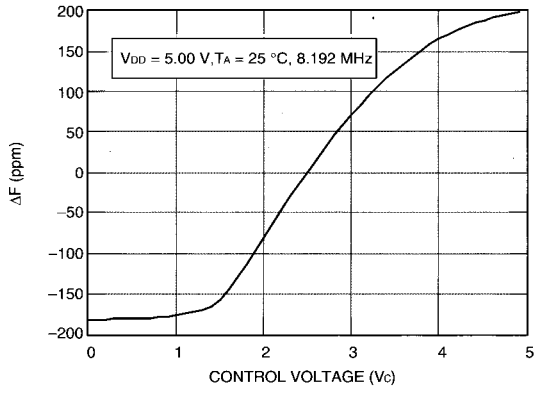


Figure 11. Output Frequency vs. Control Voltage

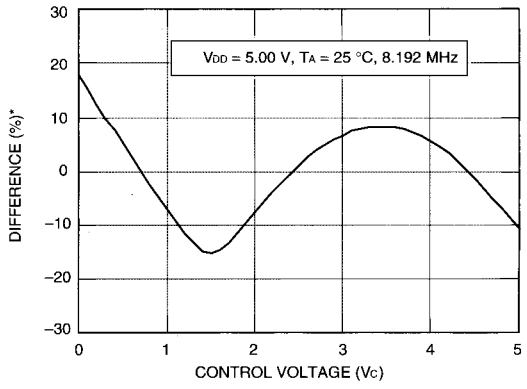


Figure 12. VCXO Linearity (Deviation From Best Linear Fit)

Table 4. Absolute Pull Range (APR)

Parameter	Symbol	Min	Max	Unit
Absolute Frequency Pull Range:	APR	-	-	ppm from f_o
Control Voltage, V_C = 0.50V for 5V	-	-APR	-	ppm from f_o
Control Voltage, V_C = 4.50V for 5V	-	+APR	-	ppm from f_o
Control Voltage, V_C = 0.30V for 3.3V	-	-APR	-	ppm from f_o
Control Voltage, V_C = 3.00V for 3.3V	-	+APR	-	ppm from f_o

Absolute pull range (APR) is specified by the fourth character of the product code (seeTable 5). The APR is the minimum guaranteed frequency shift from f_o over variations in temperature, aging, power supply, and load. Both frequency and environment limit the specified APR.

With Vc between 0.5 V and 4.5 V, total pull range for the V-Type VCXO is typically between 200 ppm and 400 ppm. A 50 ppm APR V-Type VCXO will fully track a 50 ppm source oscillator or other 50 ppm reference under all specified environmental conditions.

Table 5. Mechanical and Environmental Compliance

Parameter	Conditions
Mechanical Shock	MIL-STD-883C, 2002.3 B
Mechanical Vibration	MIL-STD-883C, 2007.1 A
Lead Solderability	MIL-STD-883C, 2003.5
Gross Leak	MIL-STD-883C, 1014.7
Fine Leak	MIL-STD-883C, 1014.7
StorageTemperature	-55 °C to 125 °C

Oscillator Aging

Quartz stabilized oscillators typically exhibit a change in output frequency with age. The major factors that contribute to this change are variations in the mechanical stress applied to the quartz crystal and mass-loading of foreign material upon the quartz crystal.

As the oscillator ages, relaxation of the crystal's mounting stress can lead to frequency variation. In some oscillator products, additional variations may be brought about by the transfer of external environmental stress through the device package and crystal mounting arrangement. VI has minimized these two effects through the use of a state-of-the-art miniature AT-Cut rectangular resonator. This crystal allows a mounting arrangement that results in minimal relaxation and very little environmental stress transfer.

Mass-loading of the quartz resonator, which generally drives the frequency lower, is a result of outgassing of materials within a hermetic package or contamination from external materials in a less than hermetic device. In general, higher frequency resonators are more susceptible to this aging mechanism. VI has minimized the V-Type's sensitivity to these effects by ensuring the hermetic integrity of the package design and by minimizing the parts count in the device. By using monolithic IC technology, the component count is reduced and the amount of material likely to outgas is minimized.

Under normal operating conditions with an operating temperature of 40°C, the V-Type VCXO will typically exhibit 2ppm aging in its first year of operation.The device is then expected to exhibit 1ppm aging the following year and will continue a logarithmic decline for each year there after.

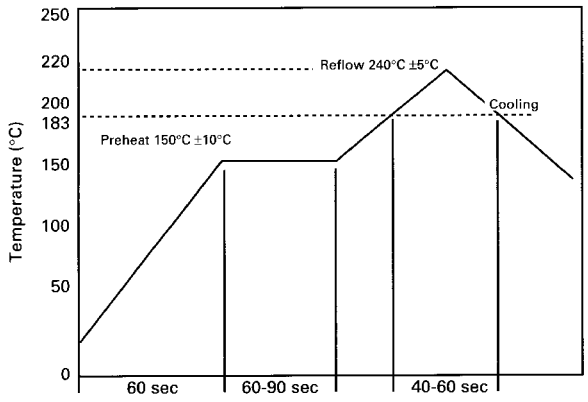


Figure 13. Recommended Solder Reflow Profile

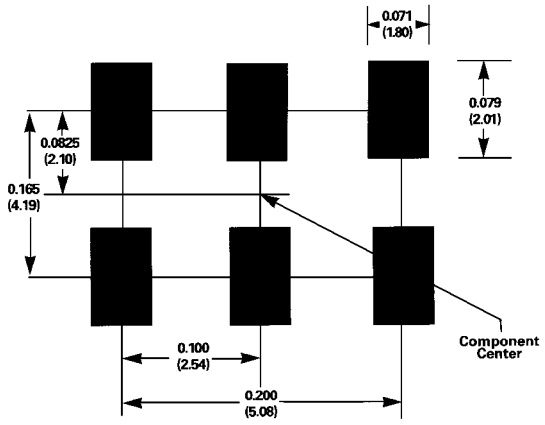


Figure 14. Recommended Solder Pad Layout

Mechanical Characteristics (continued)

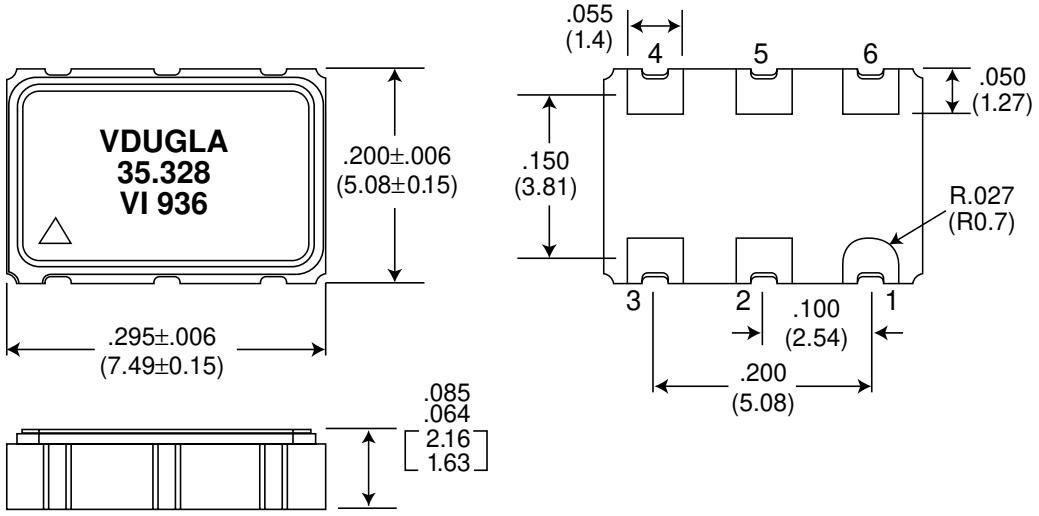


Figure 15. Package Outline Drawing

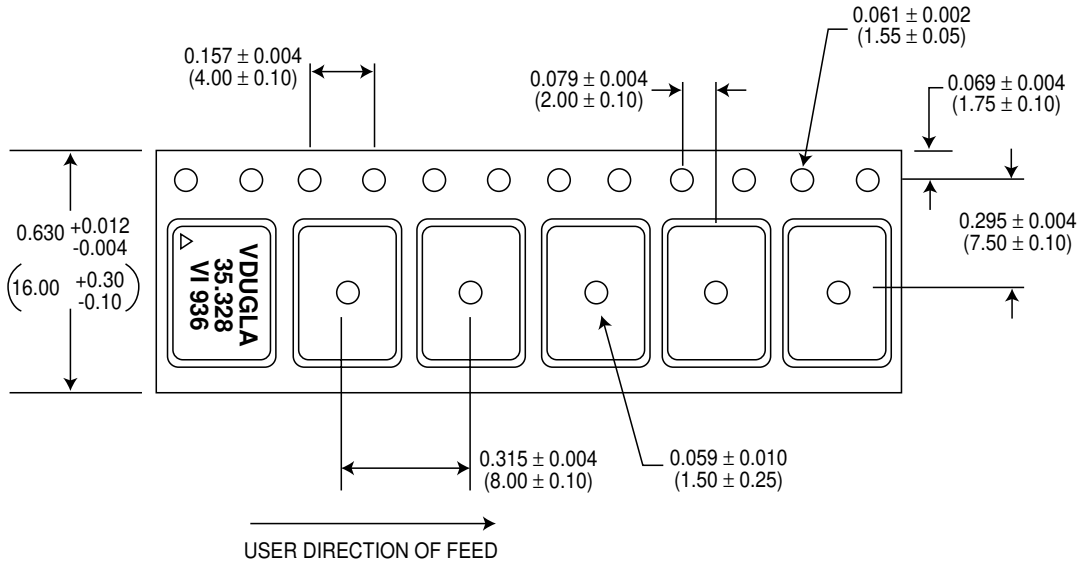


Figure 16. Carrier Tape Specifications
(Top view with tape removed - 500 devices per reel)

Dimensions are in inches and (millimeters)

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. VI employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the mode. Although no industry-wide standard has been adopted for the CDM, a standard HBM (resistance = 1500Ω, capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes. The HBM ESD threshold presented here was obtained by using these circuit parameters.

Table 6. ESD Threshold Voltage

Model	ESD Threshold, Minimum	Units
Human Body Model	1500*	V
Charged Device Model	1500	V

* MIL-STD-883D, Method 3015, Class 1

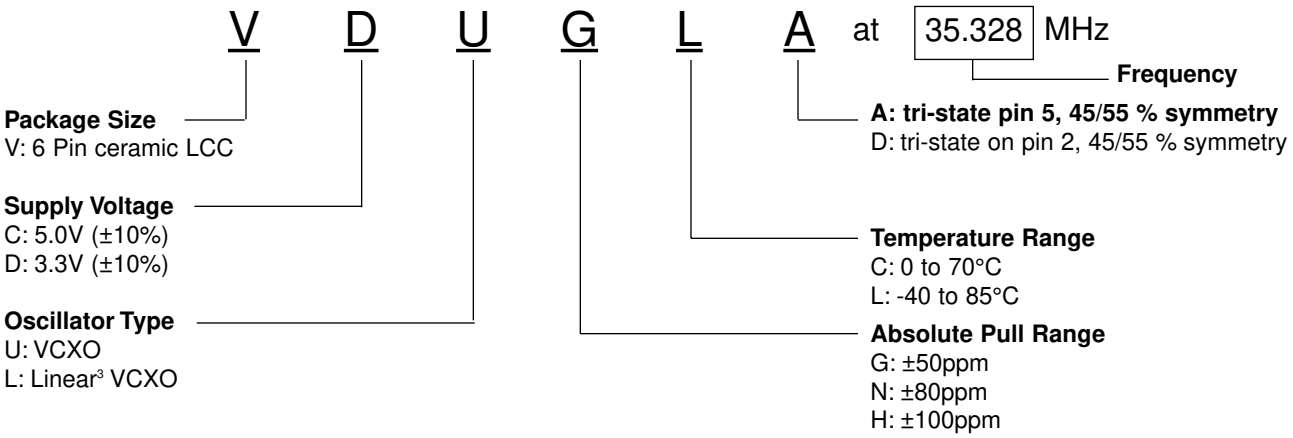
Ordering Information

Table 7: Standard Frequencies* (MHz)

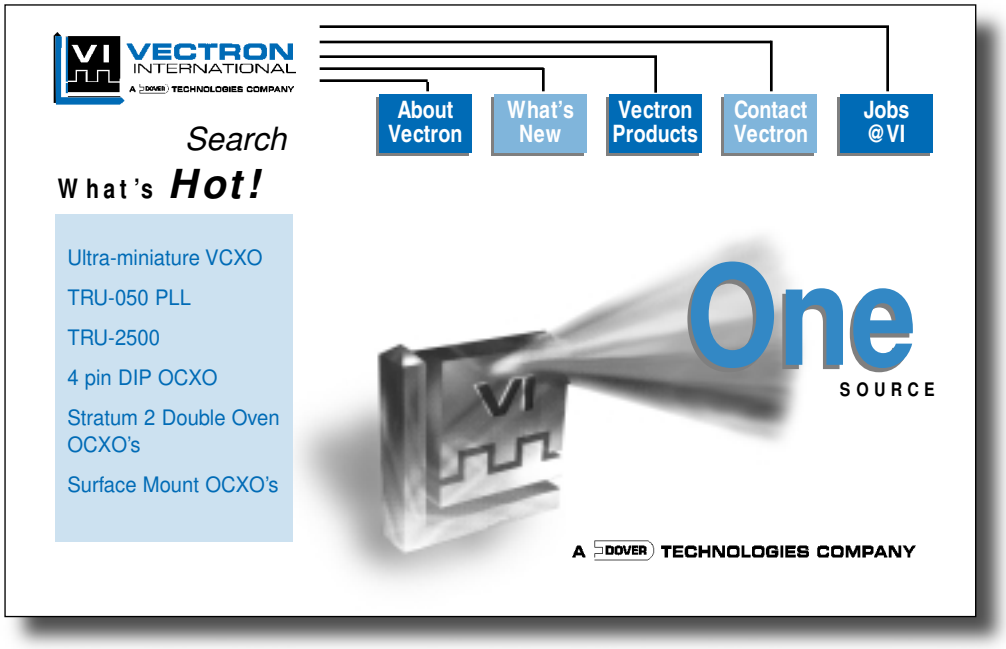
1.024	1.544	2.000	2.048	3.088	3.580
3.686	4.000	4.032	4.096	4.434	5.000
6.144	6.176	6.312	6.400	8.000	8.192
8.448	10.000	12.000	12.288	12.352	13.000
14.318	15.360	15.440	16.000	16.384	18.432
19.44	20.000	20.480	24.000	24.576	24.704
27.000	30.000	32.000	32.768	34.368	35.328
38.880	40.000	40.960	44.736	50.000	51.840
52.000	65.536	77.760			

***Other frequencies available upon request**

Table 8: Part Numbering



1. Not all combinations are possible. Other specifications may be available upon request.
2. Frequency: in MHz with decimal point, in Hz if no decimal is present.
3. 10% linearity available at certain frequencies. Consult factory.



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